IAT 2

* Required

1. Email address *

2. Name *

3. USN *

4. Section *

Mark only one oval.

- A
- B
- E

5. DMA controller must decrement the memory address for successive words 2 points

Mark only one oval.

- Yes
- No

6. Exclusive access of main memory given to DMA to transfer block of data without interruption is known as 2 points

Mark only one oval.

- Burst Mode
- Cycle Mode

7. What is the need for synchronization between I/O and processor data transfers? 2 points

Mark only one oval.

- Difference in speed
- Difference in location
- Difference in size
- Difference in memory

8. Registers DATAIN and DATAOUT along with status flags SIN and SOUT belongs to... 2 points

Mark only one oval.

- Program Interface
- Device Interface
- Bus Interface
- None

9. Memory Mapped I/O is the one in which 2 points

Mark only one oval.

- some peripheral device registers are referred by unknown addresses
- some memory address values are not used to refer peripheral device registers
- some memory address values are used to refer to peripheral device buffer registers
- None

10. A list of data elements with the accessing restriction that elements can be added or removed at one end of the list only is called 2 points

Mark only one oval.

- Pushup Stack
- Pushdown Stack
- Bottom-up Stack
- None

11. Stack pointer is 1 point

Mark only one oval.

- A processor register used to keep track of address of the top element of the stack
- A processor register used to keep track of address of the bottom element of the stack
- A processor register used to keep track of address of no element of the stack
- All of them

12. Call instruction performs 2 points

Check all that apply.

- [ ] Storing the contents of the PC in the link register
- [ ] Branch to the address contained in the link register
- [ ] Branch to the target address specified by the instruction
- [ ] All of them

13. Exchange of information between a calling program and a subroutine is referred to as 1 point

Mark only one oval.

- ◯ Information Passing
- ◯ Parameter Passing

14. When the calling program passes the parameter to the subroutine using address, the technique is called 2 points

Mark only one oval.

- ◯ Passed by value
- ◯ Passing by reference

15. Result of the instruction AShiftR #3, R0, where R0 contains 3D h is 4 points

Mark only one oval.

- ◯ 1F
- ◯ 0F
- ◯ FF
- ◯ 07

16. When you rotate the contents of R0=A5 h, five times, with and without carry, assuming CARRY=1 in both the cases, the results will be respectively... 5 points

Mark only one oval.

- BA h and B4 h with CARRY=1 in both the cases
- A2 h and A7 h with CARRY=0 in both the cases
- A2 h and A7 h with CARRY=1 in both the cases
- BA h and B4 h with CARRY=0 in both the cases

17. The processor repeatedly checks a status flag to achieve the required synchronization between the processor and an I/O device. This is 2 points

Mark only one oval.

- Memory Mapped I/O
- Program Controlled I/O

18. A hardware signal used by the I/O devices to alert the processor when they become ready is called 2 points

Mark only one oval.

- Interrupt
- Interrupt Request Line
- All of them
- None

19. The routine executed in response to an interrupt is called 1 point

Mark only one oval.

- ◯ Sub-service routine
- ◯ Interrupt-service routine

20. INTA signal is used to acknowledge 1 point

Mark only one oval.

- ◯ interrupted device
- ◯ interrupting device

21. Interrupt Latency is 2 points

Mark only one oval.

- ◯ the delay incurred between the arrival time of INTA and start of the execution of the ISR
- ◯ the delay incurred before the arrival time of INTR
- ◯ the delay incurred between the arrival time of INTR and start of the execution of the ISR
- ◯ the delay incurred before the arrival time of INTA
- ◯ Other: _____

22. Choose the correct order while handling interrupt request from a single device 1. The device is informed that the request has been recognized and in response deactivates the interrupt-request signal. 2. Interrupts are enabled and the execution of interrupted program is being resumed. 3. The processor interrupts the program currently being executed. 4. The device raises an interrupt request. 5. Interrupts are disabled by changing the control bits in the PS register. 6. The action requested by the interrupt is being performed by the interrupt service routine. 4 points

Mark only one oval.

- 4, 3, 1, 5, 6, 2
- 3, 4, 5, 1, 2, 6
- 3, 4, 5, 1, 6, 2
- 4, 3, 5, 1, 6, 2

23. Vectored Interrupts are 1 point

Mark only one oval.

- starting address of the ISR
- ending address of the ISR