USN

Internal Assessment Test 2 – Oct. 2020 (Scheme & Solution)

Sub:	POWER ELECTRONICS			Sub Code:	17EC73 & 15EC73	Branch:	ECE
Date:	05-11-2020 (Thursday)	Duration:	90 mins (2pm to 3.30pm)	Max Marks:	50	Sem / Sec	7th Sem, Sections - A, B, C, D.

		OBE	
Answer any FIVE FULL Questions	MARKS	CO	RBT
1 With a neat circuit diagram and wave forms explain the working of a single phase fully controlled converter with inductive load and continuous load current, also derive the expressions for average output voltage and rms output voltage.	10	CO5	L2

Soln.

- The circuit arrangement of a single-phase full converter is shown in Figure10.1a with a highly inductive load.
- This enables load current to be continuous and ripple free.
- During the positive half cycle, thyristors T_1 & T_2 are forward biased.
- When these 2 thyristors are turned on simultaneously at ωt = α, the load is connected to the input supply through T_1 & T_2.
- Due to the inductive load, thyristors T_1 & T_2 continue to conduct beyond ωt = π, even though the input voltage is already negative.

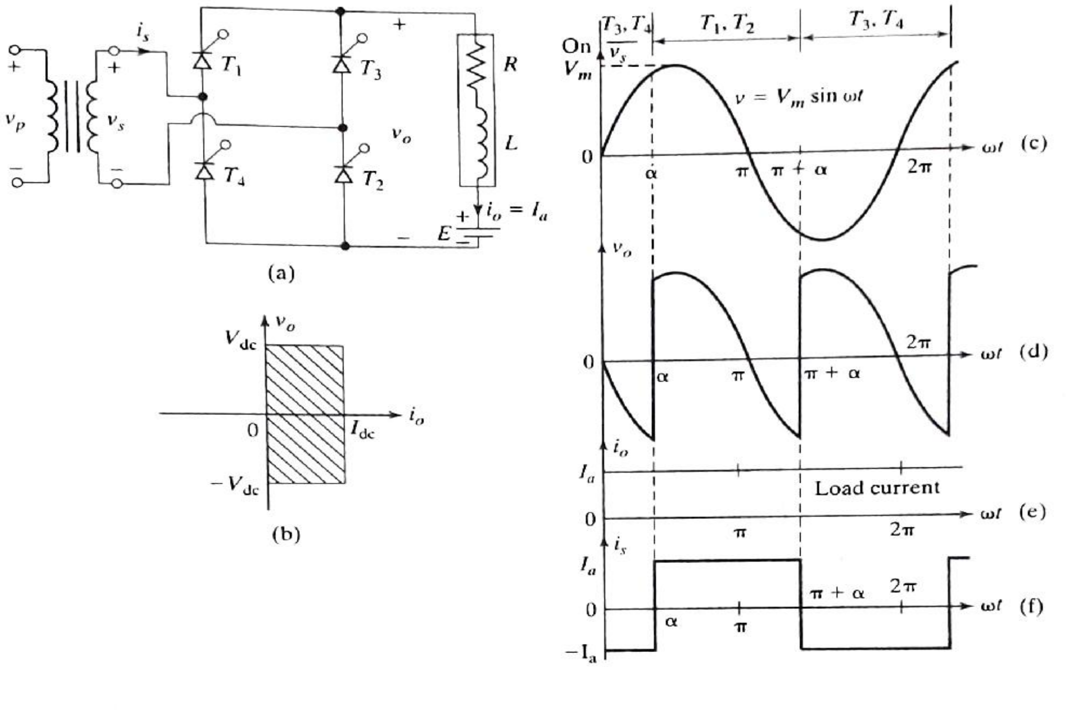


FIGURE 10.1

Single-phase full converter. (a) Circuit, (b) Quadrant, (c) Input supply voltage, (d) Output voltage, (e) Constant load current, and (f) Input supply current.

- During the negative half-cycle of the input voltage, thyristors T_3 & T_4 are forward biased.
- The turning on of thyristors T_3 & T_4 applies the supply voltage across thyristors T_1 & T_2 as reverse blocking voltage.
- T_1 & T_2 are turned off due to **line or natural commutation** & the load current is transferred from T_1 & T_2 to T_3 & T_4.
- Figure 10.1b shows the regions of converter operation.
- Figures 10.1c-f show the waveforms for input voltage, output voltage, & input and output currents.
- During the period from α to π, the input voltage v_s & input current i_s are positive, & power flows from the supply to the load.
- The converter is said to be operated in **rectification** mode.
- During the period from π to π + α, the input voltage v_s is negative & the input current i_s is positive.
- Hence, reverse power flows from the load to the supply.
- The converter is said to be operated in **inversion mode**.
- This converter is extensively used in industrial applications up to 15 kW.
- Depending on the value of α, the average output voltage could be either positive or negative, & it provides 2-quadrant operation.

The average output voltage can be found from

$$V_{dc} = \frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d(\omega t) = \frac{2V_m}{2\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{2V_m}{\pi}\cos\alpha \tag{10.1}$$

and V_{dc} can be varied from $2V_m/\pi$ to $-2V_m/\pi$ by varying α from 0 to π. The maximum average output voltage is $V_{dm} = 2V_m/\pi$ and the normalized average output voltage is

$$V_n = \frac{V_{dc}}{V_{dm}} = \cos\alpha \tag{10.2}$$

The rms value of the output voltage is given by

$$V_{rms} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2} = \left[\frac{V_m^2}{2\pi}\int_{\alpha}^{\pi+\alpha}(1-\cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2}} = V_s \tag{10.3}$$

With a purely resistive load, thyristors T_1 and T_2 can conduct from α to π, and thyristors T_3 and T_4 can conduct from $\alpha + \pi$ to 2π.

Circuit Figure & Waveforms = 5 Marks, Explanation & Equations = 5 marks.

2 With a neat diagram and waveforms, explain the principle of operation of dual converter, with and without circulating current. 10 CO5 L3

Soln.

Circuit Figure & Waveforms = 5 Marks, Explanation & Equations = 5 marks.

- Single-phase full converters with inductive loads allow only a two-quadrant operation.
- 2 of these full converters are connected back to back, as shown in Figure 10.2a.
- This enables both the output voltage and the load current flow to be reversed.
- Thus, the system provides a 4-quadrant operation & is called a **dual converter**.
- Dual converters are normally used in high-power variable-speed drives.
- If α_1 and α_2 are the delay angles of converters 1 and 2, respectively, the corresponding average output voltages are V_{dc1} and V_{dc2}.
- The delay angles are controlled.
- This is done such that one converter operates as a rectifier & the other converter operates as an inverter.
- But, both converters produce the same average output voltage.
- Figures 10.2b-f show the output waveforms for 2 converters, where the 2 average output voltages are the same.
- Figure 10.2b shows the V-I characteristics of a dual converter.

From Eq. (10.1) the average output voltages are

$$V_{dc1} = \frac{2V_m}{\pi} \cos \alpha_1 \tag{10.11}$$

and

$$V_{dc2} = \frac{2V_m}{\pi} \cos \alpha_2 \tag{10.12}$$

Because one converter is rectifying and the other one is inverting,

$$V_{dc1} = -V_{dc2} \quad \text{or} \quad \cos \alpha_2 = -\cos \alpha_1 = \cos(\pi - \alpha_1)$$

Therefore,

$$\alpha_2 = \pi - \alpha_1 \tag{10.13}$$

Because the instantaneous output voltages of the two converters are out of phase, there can be an instantaneous voltage difference and this can result in circulating current between the two converters. This circulating current cannot flow through the load and is normally limited by a *circulating current reactor* L_r, as shown in Figure 10.2a.

If v_{o1} and v_{o2} are the instantaneous output voltages of converters 1 and 2, respectively, the circulating current can be found by integrating the instantaneous voltage difference starting from $\omega t = \pi - \alpha_1$. Because the two average output voltages during the interval $\omega t = \pi + \alpha_1$ to $2\pi - \alpha_1$ are equal and oppositive, their contributions to the instantaneous circulating current i_r is zero.

$$
\begin{aligned}
i_r &= \frac{1}{\omega L_r}\int_{\pi-\alpha_1}^{\omega t} v_r\, d(\omega t) = \frac{1}{\omega L_r}\int_{\pi-\alpha_1}^{\omega t} (v_{o1} + v_{o2})\, d(\omega t) \\
&= \frac{V_m}{\omega L_r}\left[\int_{2\pi-\alpha_1}^{\omega t} \sin \omega t\, d(\omega t) - \int_{2\pi-\alpha_1}^{\omega t} -\sin \omega t\, d(\omega t)\right] \\
&= \frac{2V_m}{\omega L_r}(\cos \alpha_1 - \cos \omega t) \quad i_r > 0 \quad \text{for} \quad 0 \le \alpha_1 < \frac{\pi}{2} \qquad (10.14) \\
&\qquad\qquad\qquad\qquad\qquad\quad\; i_r < 0 \quad \text{for} \quad \frac{\pi}{2} < \alpha_1 \le \pi
\end{aligned}
$$

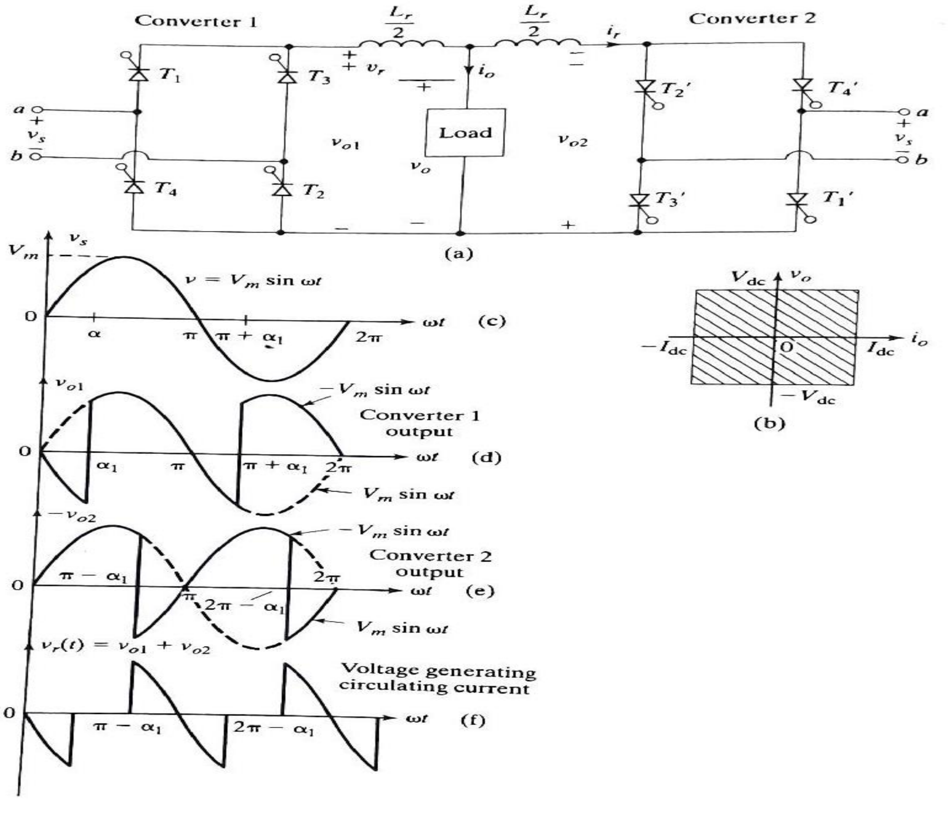
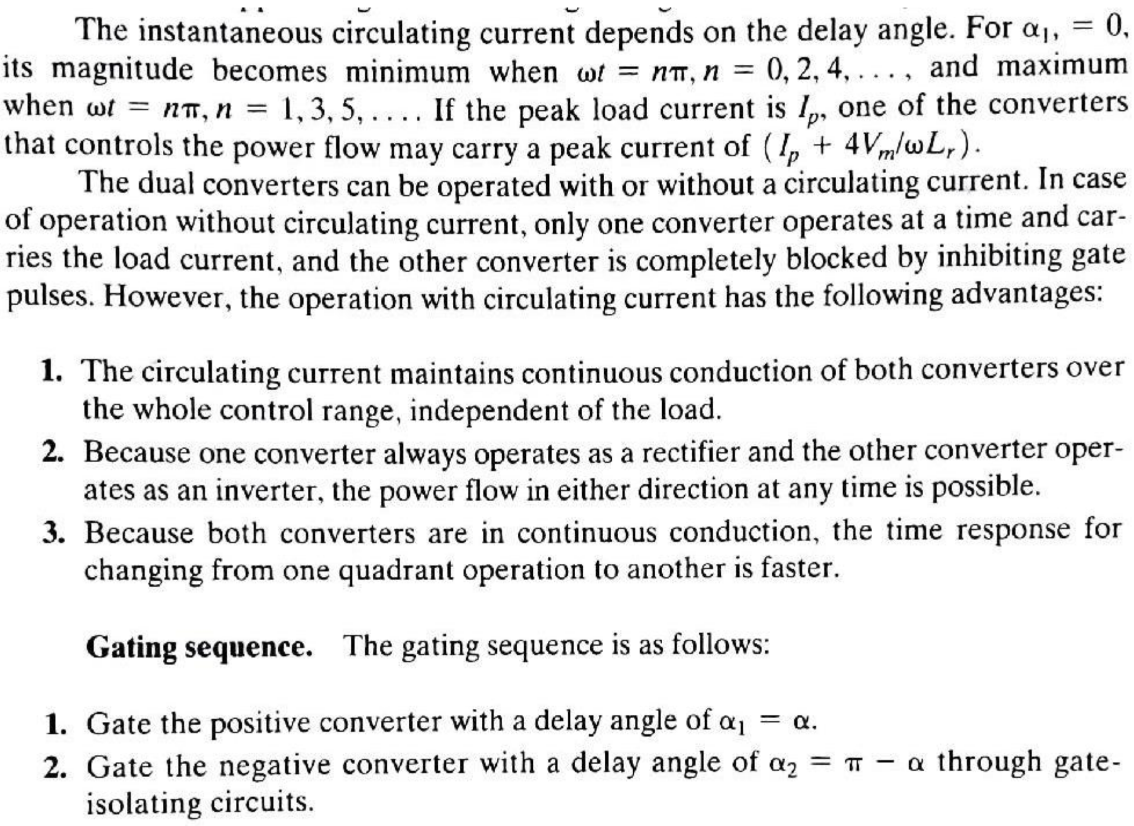


FIGURE 10.2
Single-phase dual converter. (a) Circuit, (b) Quadrant, (c) Input supply voltage, (d) Output voltage for converter 1, (e) Output voltage for converter 2, and (f) Circulating inductor voltage.

- For α_1=0, only the converter 1 operates ; for α_1=π, only the converter 2 operates.

- For $0 \le \alpha_1 < \pi/2$, the converter 1 supplies a positive load current $+i_o$.
- Thus, the circulating current can only be positive.
- For $\pi/2 < \alpha_1 \le \pi$, the converter 2 supplies a negative load current $-i_o$.
- Thus, only a negative circulating current can flow.
- At $\alpha_1 = \pi/2$, the converter 1 supplies positive circulating during the 1st half-cycle.
- Converter 2 supplies negative circulating during the second half-cycle.



The instantaneous circulating current depends on the delay angle. For $\alpha_1, = 0$, its magnitude becomes minimum when $\omega t = n\pi, n = 0, 2, 4, \ldots$, and maximum when $\omega t = n\pi, n = 1, 3, 5, \ldots$. If the peak load current is I_p, one of the converters that controls the power flow may carry a peak current of $(I_p + 4V_m/\omega L_r)$.

The dual converters can be operated with or without a circulating current. In case of operation without circulating current, only one converter operates at a time and carries the load current, and the other converter is completely blocked by inhibiting gate pulses. However, the operation with circulating current has the following advantages:

1. The circulating current maintains continuous conduction of both converters over the whole control range, independent of the load.
2. Because one converter always operates as a rectifier and the other converter operates as an inverter, the power flow in either direction at any time is possible.
3. Because both converters are in continuous conduction, the time response for changing from one quadrant operation to another is faster.

Gating sequence. The gating sequence is as follows:

1. Gate the positive converter with a delay angle of $\alpha_1 = \alpha$.
2. Gate the negative converter with a delay angle of $\alpha_2 = \pi - \alpha$ through gate-isolating circuits.

10	CO5	L2

3 Draw the circuit diagram of a single phase AC voltage controller and explain the principle of ON-OFF control, with the help of relevant waveforms. Derive the expression for rms output voltage in terms of rms supply voltage and duty cycle of the operation of the controller.

Soln.

Circuit Figure & Waveforms = 5 Marks, Explanation & Equations = 5 marks.

- If a thyristor switch is connected between ac supply & load, the power flow can be controlled.
- This is done by varying the rms value of ac voltage applied to the load.
- This type of power circuit is known as an **ac voltage controller**.
- The most common applications of ac voltage controllers are :

✓ Industrial heating

✓ On-load transformer connection changing

✓ Light controls

- ✓ Speed control of polyphase induction motors, and,
- ✓ AC magnet controls.

- For power transfer, 2 types of control are normally used :

1) **On-off control**
2) **Phase-angle control**

- A single phase full-wave controller with a resistive load is shown in Figure 11.2a.
- During the positive half-cycle of input voltage, the power flow is controlled by varying the delay angle of thyristor T_1.
- Thyristor T_2 controls the power flow during the negative half-cycle of input voltage.
- The firing pulses of T_1 & T_2 are kept 180^o apart.
- The waveforms for the input voltage, output voltage, & gating signals for T1 & T2 are shown in Figure 11.2b-e.

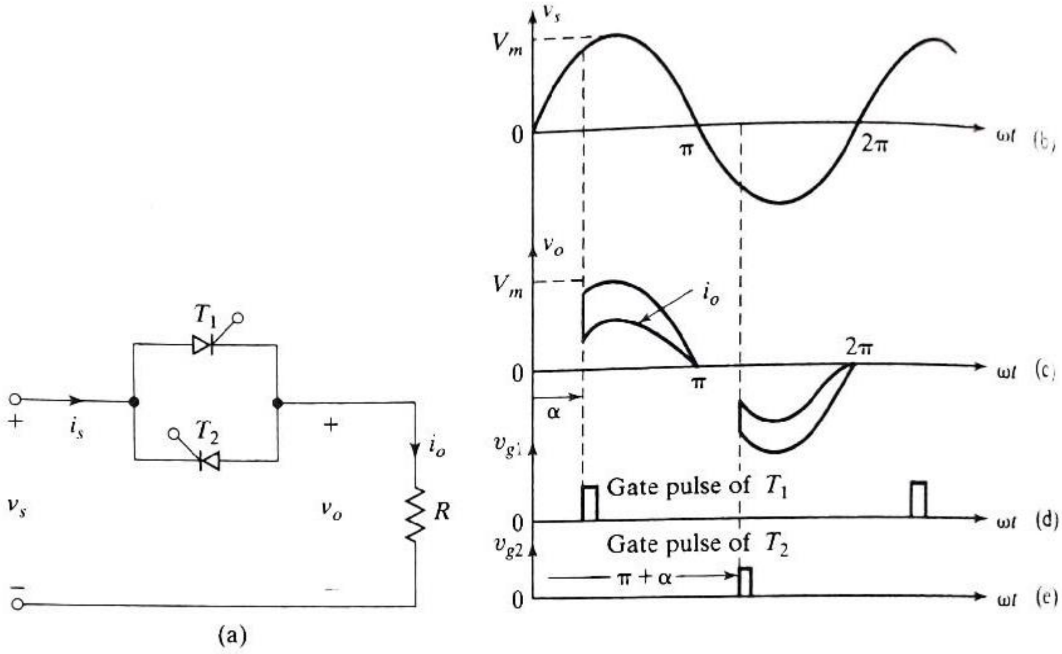
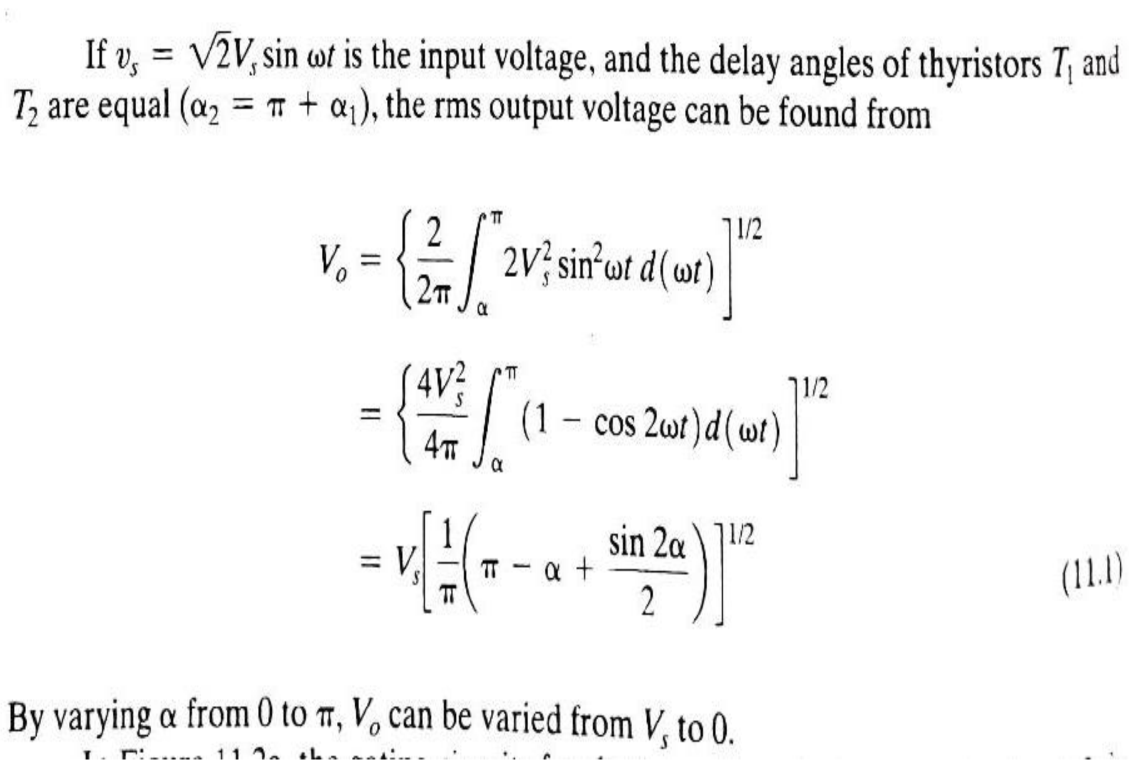


FIGURE 11.2

Single-phase full-wave controller. (a) Circuit, (b) Input supply voltage, (c) Output voltage, (d) Gate pulse for T_1, and (e) Gate pulse for T_2.



If $v_s = \sqrt{2}V_s \sin \omega t$ is the input voltage, and the delay angles of thyristors T_1 and T_2 are equal ($\alpha_2 = \pi + \alpha_1$), the rms output voltage can be found from

$$V_o = \left\{ \frac{2}{2\pi} \int_{\alpha}^{\pi} 2V_s^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$= \left\{ \frac{4V_s^2}{4\pi} \int_{\alpha}^{\pi} (1 - \cos 2\omega t) d(\omega t) \right]^{1/2}$$

$$= V_s \left[\frac{1}{\pi} \left(\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2} \tag{11.1}$$

By varying α from 0 to π, V_o can be varied from V_s to 0.

4	Draw a neat sketch of 1- φ AC voltage full controller with R and RL load and explain its working. Soln. 3 circuits & explanation with R load = 3*2=6 marks, 1 circuit & explanation with RL Load= 4 marks.	10	CO5	L3

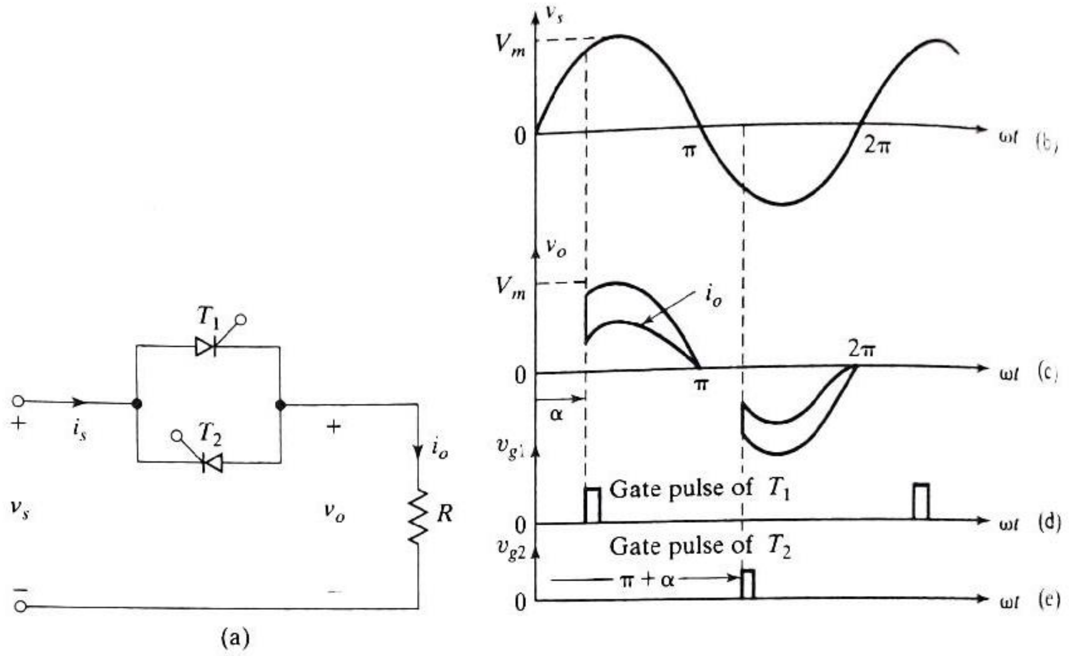


FIGURE 11.2

Single-phase full-wave controller. (a) Circuit, (b) Input supply voltage, (c) Output voltage, (d) Gate pulse for T_1, and (e) Gate pulse for T_2.

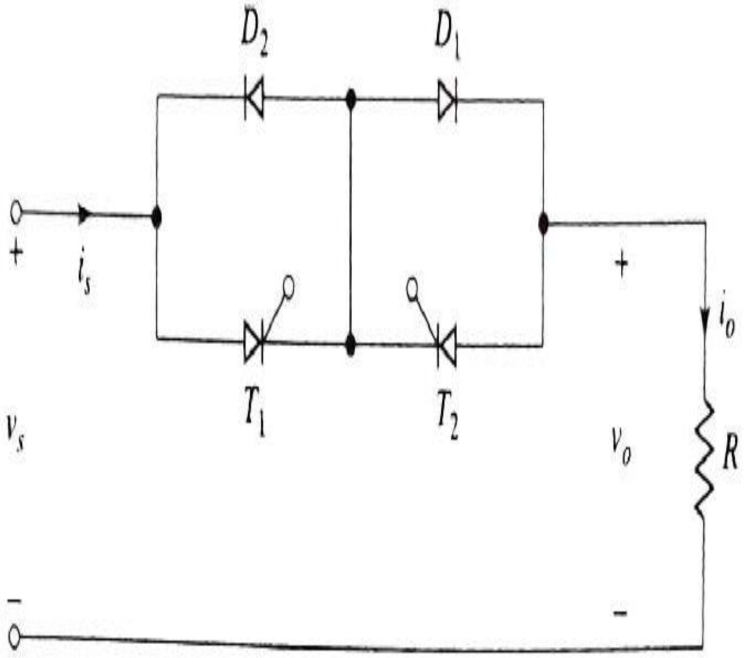


FIGURE 11.3

Single-phase full-wave controller with common cathode.

Gating sequence. The gating sequence is as follows:

1. Generate a pulse signal at the positive zero crossing of the supply voltage v_s.
2. Delay the pulse by the desired angle α for gating T_1 through a gate-isolating circuit.
3. Generate another pulse of delay angle $\alpha + \pi$ for gating T_2.

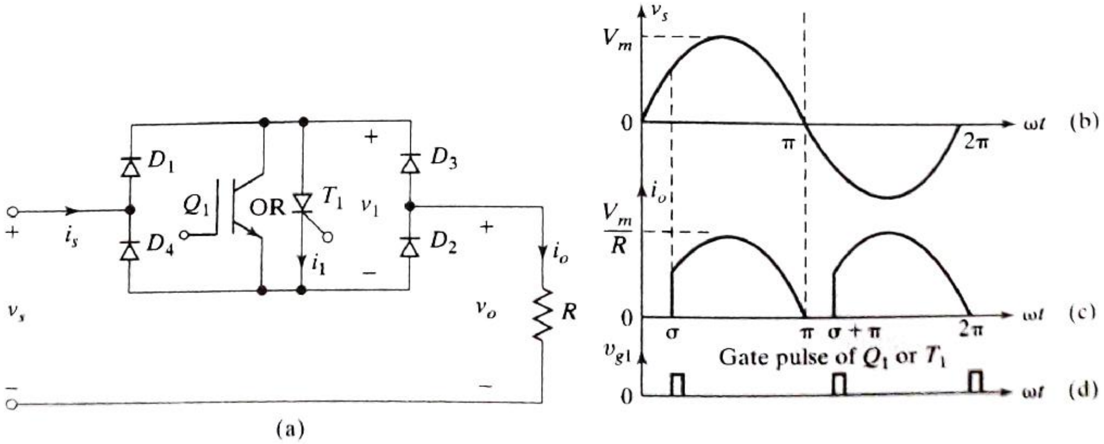


FIGURE 11.4

Single-phase full-wave controller with one thyristor. (a) Circuit, (b) Input supply voltage, (c) Output current, and (d) Gate pulse for T_1.

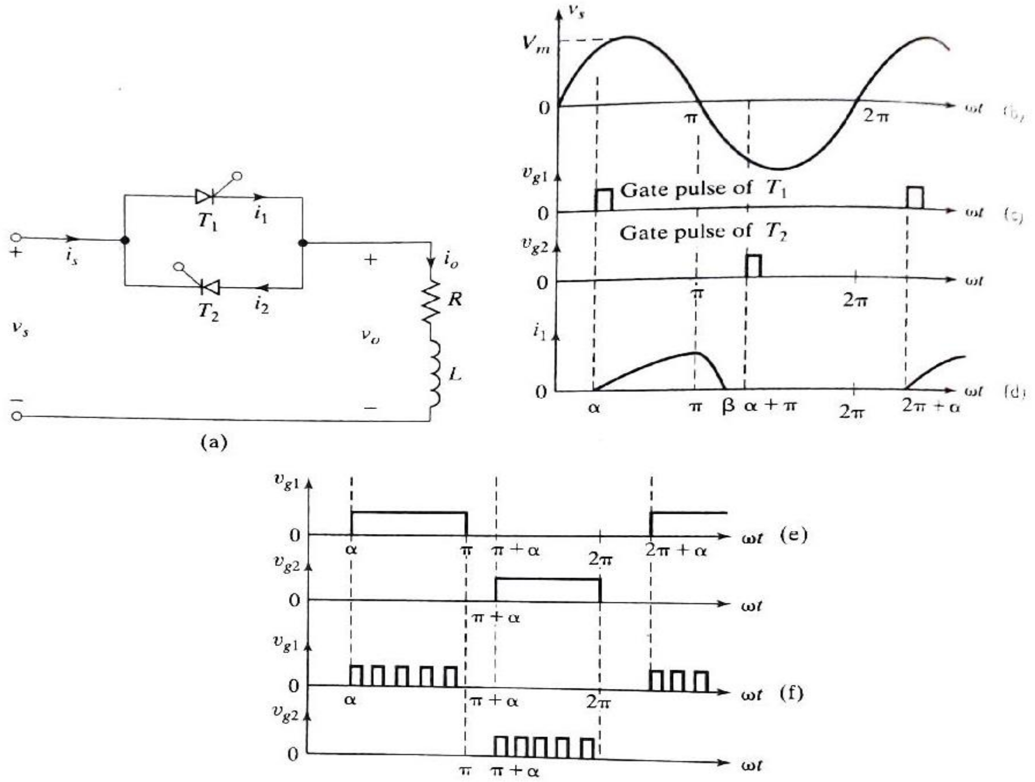


FIGURE 11.5

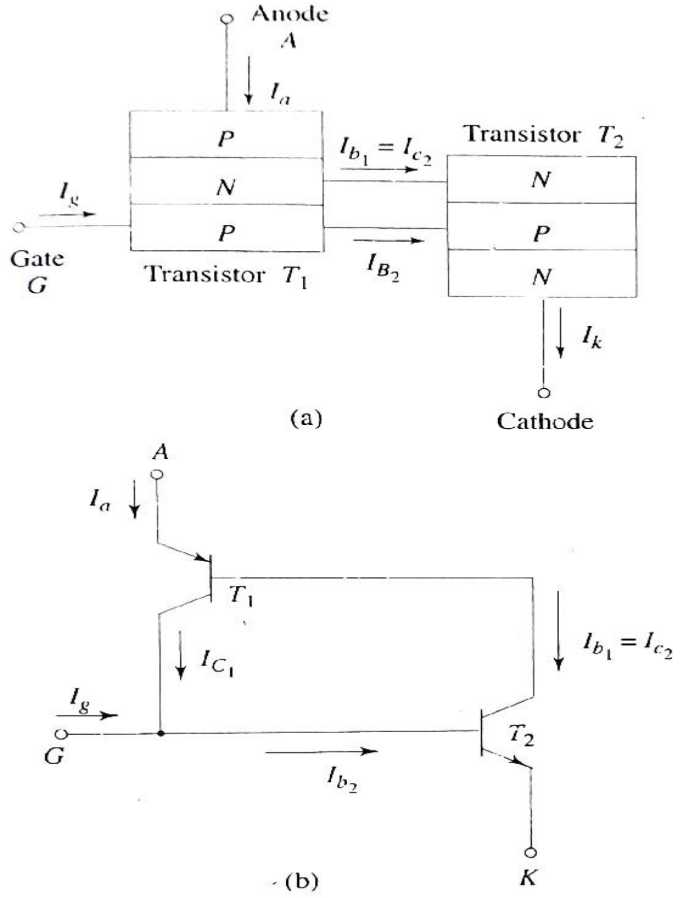
Single-phase full-wave controller with RL load. (a) Circuit, (b) Input supply voltage, (c) Gate pulses for T_1 and T_2, (d) Current through thyristor T_1, (e) Continuous gate pulses for T_1 and T_2, and (f) Train of gate pulses for T_1 and T_2.

5	Using the two transistor model, explain how a small gate current can turn on an SCR.	10	CO2	L1

Soln.

Circuit Diagram= 4 marks, Explanation & Eqns.= 6 marks.

- The operation of an SCR can be also explained in a very simple way by considering it in terms of 2 transistors.
- This is known as the 2 transistor analogy of the SCR.
- The SCR can be considered as an **npn** & a **pnp** transistor, where the collector of one transistor is attached to the base of the other & **vice-versa**, as shown in Fig.1.4.
- The model is obtained by splitting the 2 middle layers of the SCR into 2 separate parts.



I_a — Anode current
I_k — Cathode current
I_g — Gate current
I_{e_1} — Emitter current of transistor T_1 (*pnp*)
I_{b_1} — Base current of transistor T_1
I_{c_1} — Collector current of transistor T_1
I_{e_2} — Emitter-current of transistor T_2
I_{b_2} — Base-current of transistor T_2
I_{c_2} — Collector-current of transistor T_2
α_1 — Current-gain of transistor T_1
α_2 — Current-gain of transistor T_2.

Fig. 1.4 Two transistor analogy of SCR

It is observed from the figure that the collector current of transistor T_1 becomes the base current of transistor T_2 and *vice versa*.

$\therefore$ $$I_{c_1} = I_{b_2} \quad \text{and} \quad I_{b_1} = I_{c_2}$$

Also, $$I_k = I_a + I_g \tag{1.1}$$

Now, we have the relation from transistor analysis,

$$I_{b_1} = I_{e_1} - \text{I}_{c_1} \tag{1.2}$$

Also, $$I_{c_1} = \alpha_1 I_{e_1} + I_{co_1} \tag{1.3}$$

where I_{co_1} is the reverse leakage current of the reverse biased junction J_2 when the two outer layers are not present.

Substituting Eq. (1.3) in Eq. (1.2) we get

$$I_{b_1} = I_{e_1} - \alpha_1 I_{e_1} - I_{co_1}.$$

$$I_{b_1} = (I - \alpha_1) I_{e_1} - I_{co_1}$$

From Fig. 1.4, it is evident that the anode current of the device becomes the emitter current of transistor T_1 that is

$$I_a = I_{e1}$$

$\therefore$ $$I_{b_1} = (I - \alpha_1) I_a - I_{co_1} \tag{1.4}$$

Also, $$I_{c_2} = \alpha_2 I_{e_2} + I_{co_2}$$

From the Fig. 1.4, it is also observed that the cathode current of the SCR becomes the emitter-current of transistor T_2.

$\therefore$ $$I_k = I_{e_2}$$

$\therefore$ $$I_{c_2} = \alpha_2 I_k + I_{co_2} \tag{1.5}$$

But $$I_{b_1} = I_{c_2} \tag{1.6}$$

Substituting Eqs (1.4 and (1.5) in Eq. (1.6), we get

$$(1 - \alpha_1) I_a - I_{co_1} = \alpha_2 I_k + I_{co_2} \tag{1.7}$$

Substituting Eq. (1.1) in Eq. (1.7), we get

$$(1 - \alpha_1) I_a - I_{co_1} = \alpha_2 (I_a + I_g) + I_{co_2}$$

$$(1 - \alpha_1 - \alpha_2) I_a = \alpha_2 I_g + I_{co_2} + I_{co_1}.$$

$$[1 - (\alpha_1 + \alpha_2)] I_a = \alpha_2 I_g + I_{co_1} + I_{co_2}$$

$\therefore$ $$I_a = \frac{\alpha_2 I_g + I_{co_1} + I_{co_2}}{[1 - (\alpha_1 + \alpha_2)]} \tag{1.8}$$

Assuming the leakage current of transistor T_1 and T_2 to be negligible small, we have

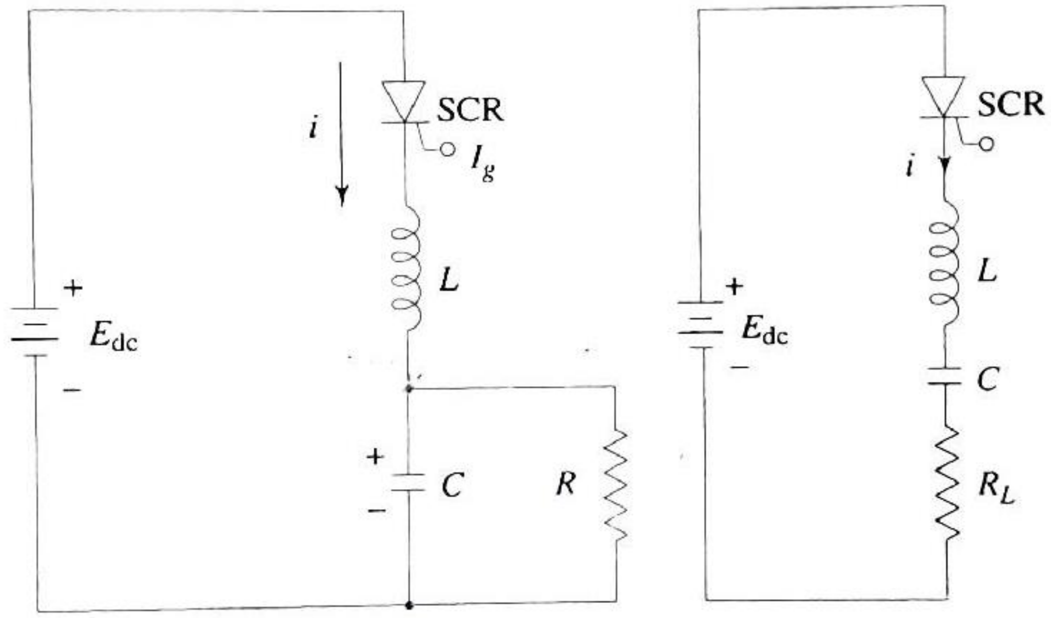
$$I_a = \frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)} \tag{1.9}$$

6	With a neat circuit diagram and wave forms explain the working of class A commutation.	10	CO2	L1

Soln.

Diagram & Waveforms= 5 marks, Explanation= 5 marks.

- This is also known as resonant commutation.
- This type of commutation circuit using L-C components-in-series-with the load are shown in Fig.1.12.
- In Fig.1.12(a), load R_L is in parallel with the capacitor & in Fig.1.12(b), load R_L is in series with the L-C circuit.
- In this process of commutation, the forward current passing through the device is reduced.
- It is reduced to less than the level of holding current of the device.
- Hence, this method is also known as the current commutation method.
- The waveforms of the thyristor voltage, current & capacitor voltages are shown in Fig.1.13.



(a) Load in parallel with capacitor

(b) Load in series with capacitor

Fig. 1.12 Class A commutation circuit

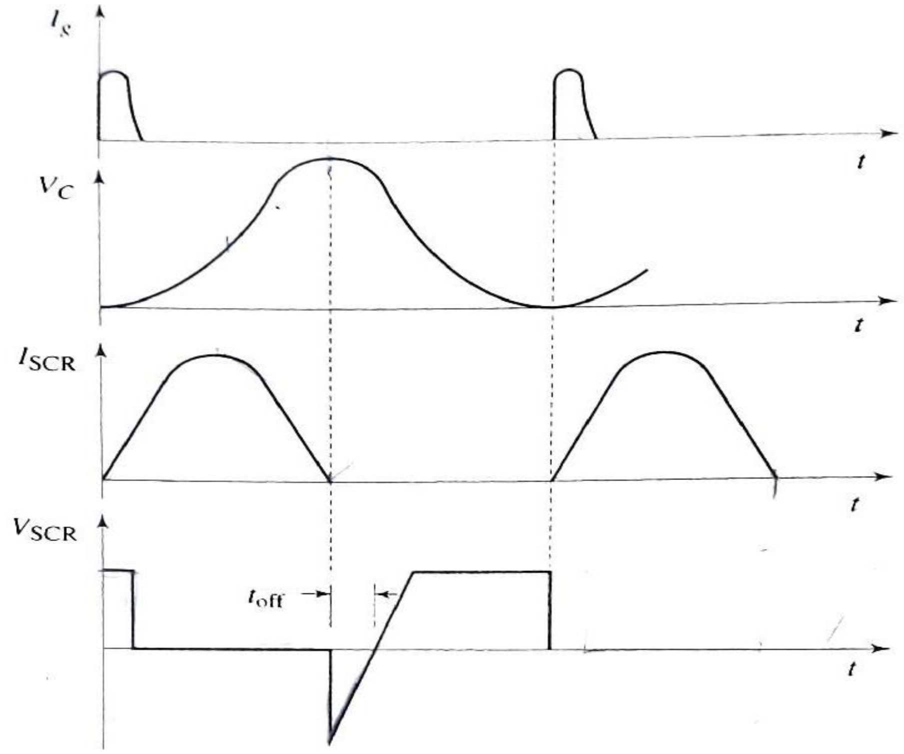
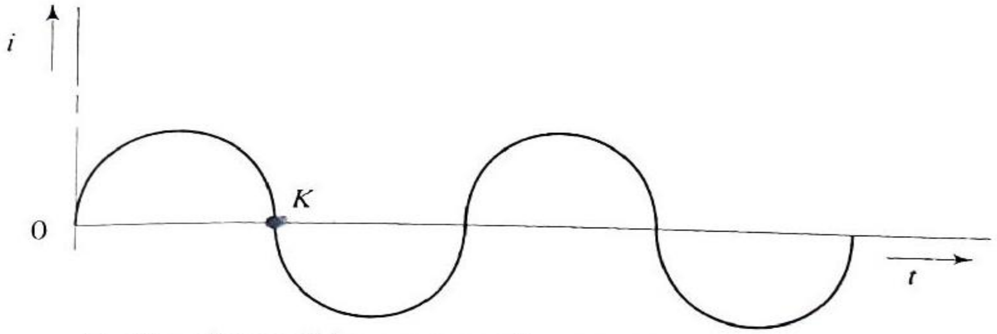
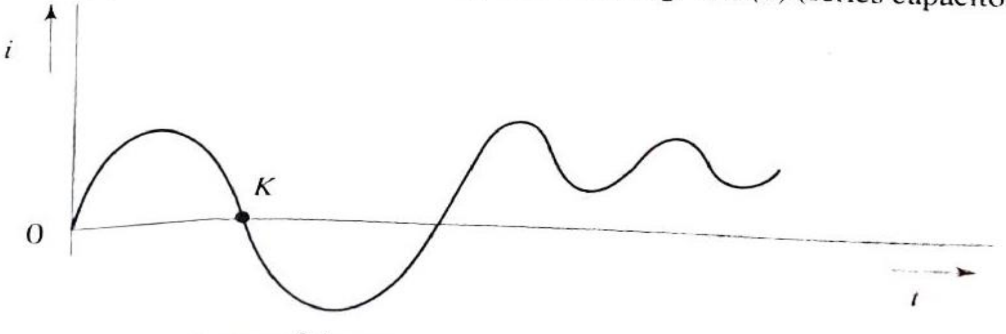


Fig. 1.13 Voltages and currents in Class A (load is parallel with capacitor)



(a) Waveforms of the current produced in Fig. 1.12(b) (series capacitor)



(b) Waveforms of the current produced in Fig. 1.12(a) (parallel capacitor)

Fig. 1.14

7 With a neat circuit diagram and wave forms explain the working of UJT triggering. 10 CO2 L2

Soln.

Circuit diagram & waveforms= 5 marks, Explanation= 5 marks.

- The unijunction transistor, abbreviated UJT, is a three-terminal, single-junction device.
- The basic UJT & its variations are essentially latching switches.
- Their operation is similar to the 4-layer diode.
- The most significant difference being that the UJT's switching voltage can be easily varied by the circuit designer.
- Like the 4-layer diode, the UJT is always operated as a switch.
- It has applications in oscillators, timing circuits & SCR/TRIAC trigger circuits.

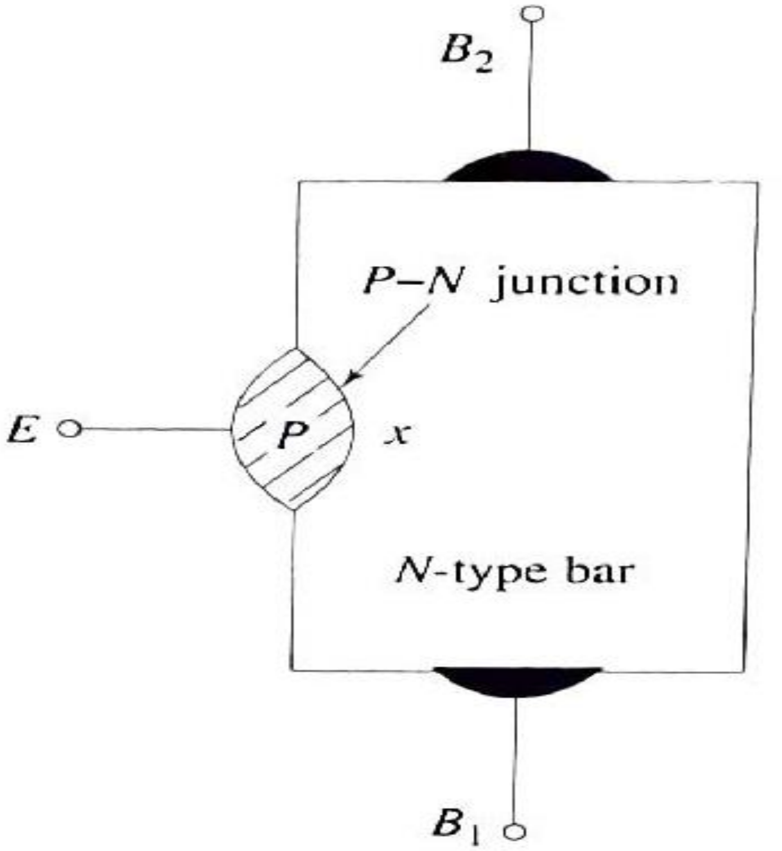


Fig. 2.14 Basic UJT structure

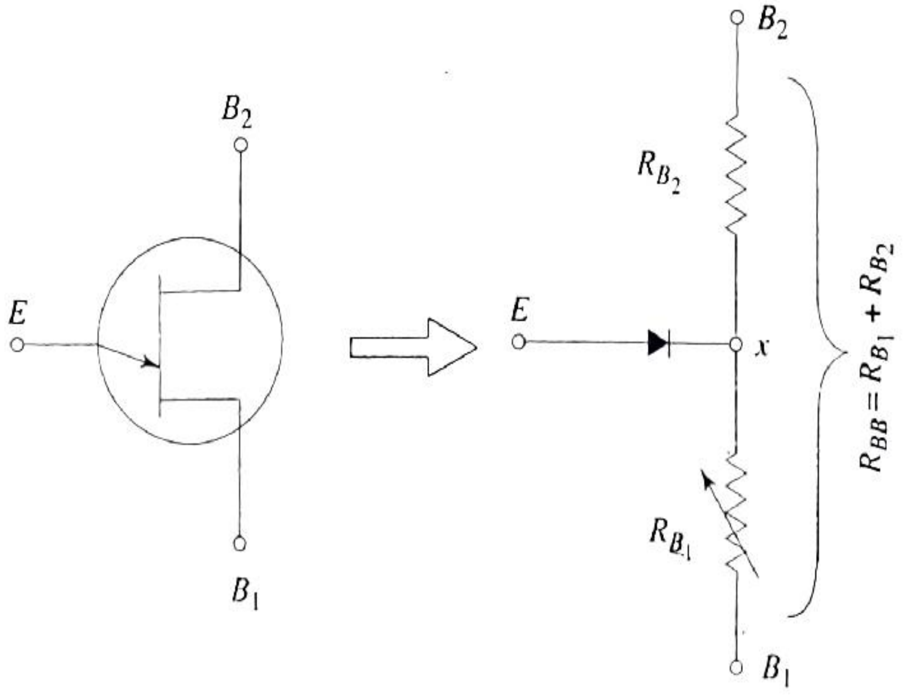


Fig. 2.15 UJT symbol and equivalent circuit

- The basic circuit is shown in Fig.2.22.
- The B_1 pulse output is used to trigger the SCR, a predetermined time after the switch is closed.
- Thus, the 1st B_1 pulse occurs T seconds after the 28 V is supplied to the UJT circuit.
- After the SCR has been triggered “on”, subsequent pulses at its gate have no effect.
- An important design consideration in this type of circuit concerns the premature triggering of the SCR.
- The voltage at B_1 when the UJT is “off”, must be smaller than the voltage needed to trigger the SCR.
- Otherwise, the SCR will be triggered immediately upon switch closure.
- Thus, we have the requirement as follows:

we have the requirement

$$V_{B_1}(\text{off}) < (I_g \times 1\ \text{k}\Omega + V_g) \tag{2.18}$$

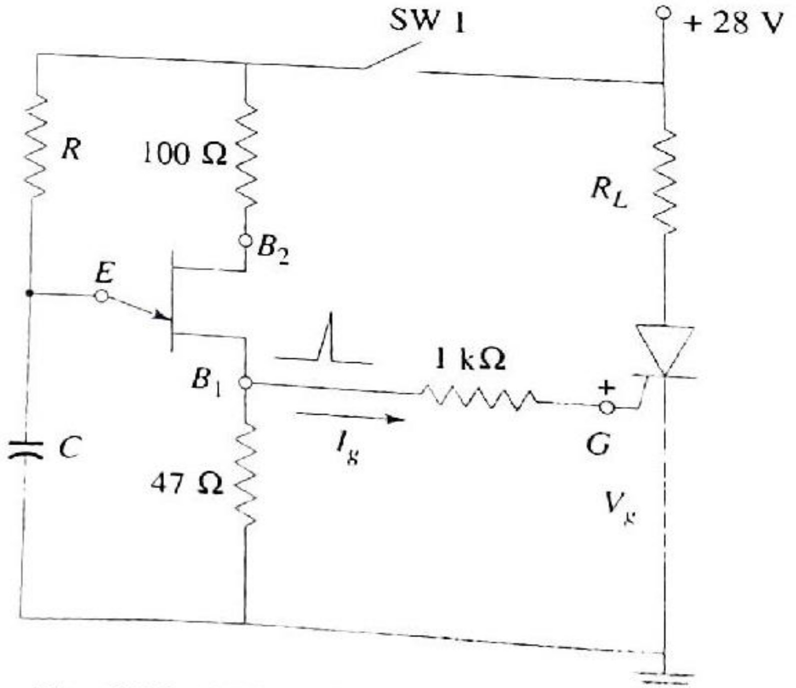


Fig. 2.22 UJT oscillator as gate trigger source

8 Explain different turn ON methods & turn off mechanism of SCR. 10 CO2 L2

Soln.

5 turn on methods & explanation= 1.5 * 5= 7.5 marks, turn off mechanism = 2.5 marks.

Turn on methods –

- Forward Voltage Triggering
- Thermal Triggering
- Radiation Triggering
- dv/dt Triggering
- Gate Triggering

Turn off mechanism –

- Once the SCR starts conducting an appreciable forward current, the gate has no control on it.
- The device can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current.
- The process of turn-off is also called as **commutation**.
- If a forward voltage is applied immediately after reducing the anode current to zero, it will not block the forward voltage.
- It will instead start conducting again, although it is not triggered by a gate pulse.
- Hence, it is necessary to keep the device reverse biased for a finite period before applying a forward anode voltage again.

- The turn-off time of the thyristor is defined as the minimum time interval between the 2 instants.
- The 1st instant is that at which the anode current becomes zero.
- The 2nd instant is that at which the device is capable of blocking the forward voltage.
- The turn-off time is illustrated by the waveforms shown in Fig.1.11.
- The total turn-off time t_{off} is divided into 2 time intervals – the reverse recovery time t_{rr} & the gate recovery time t_{gr} .

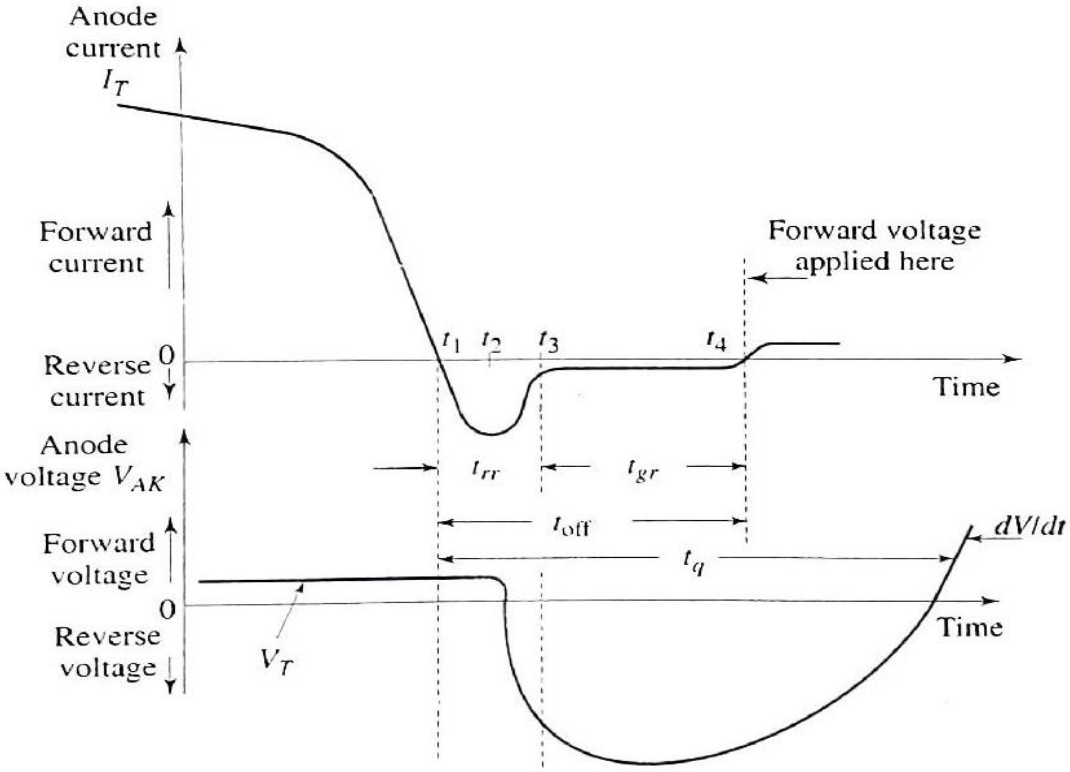


Fig. 1.11 Waveforms during SCR turn-off

- At the instant t_1, the anode forward current becomes zero.
- During the reverse recovery time, t_1 to t_3, the anode current flows in the reverse direction.
- At the instant t_2, a reverse anode voltage is developed & the reverse recovery current continues to decrease.
- At t_3, junctions J_1 & J_3 are able to block a reverse voltage.
- But, the thyristor is not yet able to block a forward voltage.
- This is because carriers, called **trapped charges**, are still present at the junction J_2.
- During the interval, t_3 to t_4, these carriers recombine.
- At t_4, the recombination is complete & hence, a forward voltage can be reapplied at this instant.
- The SCR turn-off time is the interval between t_4 & t_1.
- In an SCR, this time varies in the range 10 to 100 µs.
- Thus, the total turn-off time (t_{off}) required for the device is the sum of the 2 durations.
- The 1st duration is that for which the reverse recovery current flows after the application of reverse

voltage.

- The 2nd duration is the time required for the recombination of all excess carriers in the inner 2 layers of the device.
- In practical applications, the turn-off time required to the SCR by the circuit, called the circuit turn-off time t_q, must be greater than the device turn-off time t_{off} by a suitably safe margin.
- Otherwise, the device will turn-on at an undesired instant, a process known as **commutation failure**.
- Thyristors having large turn-off time (50-100 μs) are called as slow switching or phase control type thyristors (or converter grade thyristors).
- Those having low turn-off time (10-50 μs) are called fast switching or inverter type thyristors.
- In high frequency applications, the required circuit turn-off time consumes an appreciable portion of the total cycle time.
- Hence, for these applications, inverter grade thyristors must be used.

NOTE : ***THE QUESTIONS SHOULD BE NEATLY WRITTEN & ANSWERED IN STUDENT'S OWN HANDWRITING. ON TOP OF EACH PAGE, WRITE YOUR NAME & USN BEFORE MAKING A PDF AND UPLOADING THE PDF IN GOOGLE CLASSROOM. TOTAL TIME TAKEN SHOULD NOT EXCEED 2 HOURS FOR BOTH ANSWERING & UPLOADING THE PDF (1.5 HOURS FOR ANSWERING + 0.5 HOURS FOR UPLOADING PDF). PDF SUBMITTED AFTER 2 HOURS OR NOT AS PER THE ABOVE INSTRUCTIONS WILL NOT BE VALUATED AND MARKS ALLOTED WILL BE ZERO FOR THE TEST.***

ALL THE BEST