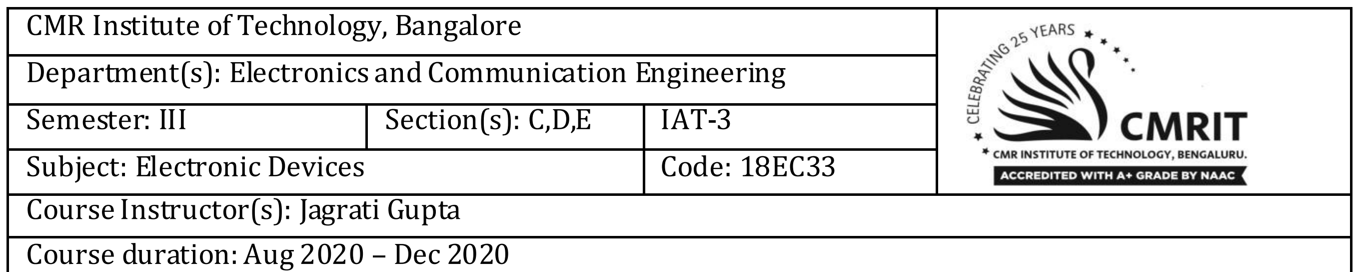


CMR Institute of Technology, Bangalore			
Department(s): Electronics and Communication Engineering			
Semester: III	Section(s): C,D,E	IAT-3	
Subject: Electronic Devices		Code: 18EC33	
Course Instructor(s): Jagrati Gupta			
Course duration: Aug 2020 – Dec 2020			

ELECTRONIC DEVICES (18EC33)

IAT-3 SCHEME AND SOLUTION

Q-1 MCQ's. --CO3 AND CO4_L2

1. Which of the following is not an advantages of IC.

Ans. Usage of long connecting wires (interconnects)

2. ___________ is a set of electronic circuits on one small flat piece of Si semiconductor material.

Ans. Monolithic IC

3. "Integration density gets almost doubled in every two years"-this statement is based on which law

Ans. Moore's law

4. In N- channel enhancement MOSFET which type (polarity) of gate voltage is applied to create the channel.

Ans. positive voltage and greater than Threshold voltage

5. For a p type MOS capacitor, if the Gate voltage is negative, then the energy bands bends___________

Ans. Upwards

6. What are the modes of operation of MOS Capacitor

Ans. All of the above

7. If Vds=Vds(sat), the drain current

Ans. Remains constant

8. In small signal equivalent model of MOSFET, where Source resistance rs is considered then the effective transconductance

Ans. Decreases compared to the case when there is no source resistance in small signal model

9. Anisotropic etchant

Ans. Only Vertically

10. What is the general sequence in PN Junction fabrication

Ans. (a) Develop oxide on Si (b) Apply photoresist (c) Photolithography (d) Etching of unwanted oxide

Q-2 Draw and explain the operation and I-V characteristics of n channel PNJFET for different biasing voltages. [10 Marks]- CO4_L2

Ans-2

Operation :-

① n-channel JFET is applied 0 V at gate.
If a small +ve drain voltage is applied, a current I_D flows between source and drain terminals.
N-channel is a resistance, so, for small V_{DS}, I_D is linear. (fig. 2(a)).

② When $V_{GS} = -ve$ $(-V_1)$, the gate to channel p-n junction gets reverse biased.
↳ space charge region widens. ⇒ channel gets narrower.
⇒ resistance of n-channel increases.
→ slope of I_D vs V_{DS} curve decreases now. (fig 2(b))

③ When $V_{GS} = -ve$ $(-V_2)$ and V_2 is more negative than V_1.
→ R.B gate to channel space charge region completely fills the channel. This condition is pinch-off.

→ The $I_D = 0$, since depletion region isolates the source and drain terminals. (fig 2(c))

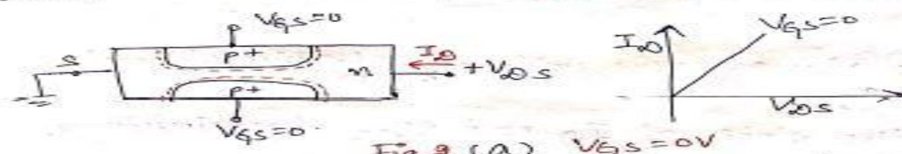


Fig 2 (a) $V_{GS} = 0V$

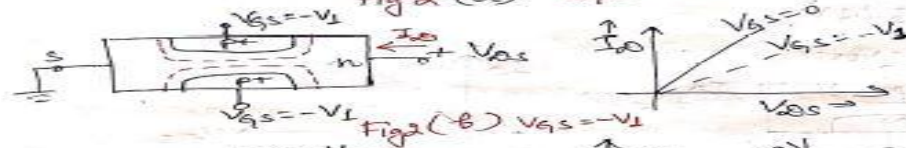


Fig 2 (b) $V_{GS} = -V_1$

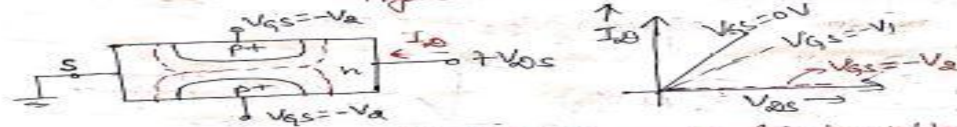


Fig 2 (c) $V_{GS} = -V_2$ (Gate voltage to achieve pinch-off)

→ The current in the channel is controlled by gate.

→ This device is normally on or depletion mode device meaning that a voltage must be applied at the gate to turn the device off.

(4) Let $V_{GS} = 0$ V and V_{DS} changes.

As V_{DS} ↑ (+ve), Gate to channel pn junction

becomes reverse biased near drain terminal so that space charge region extends further into the channel.

→ As space charge regions widens, effective channel resistance ↑.

→ Thus, the slope of I_D and V_{DS} characteristics ↓. (fig 3(b)).

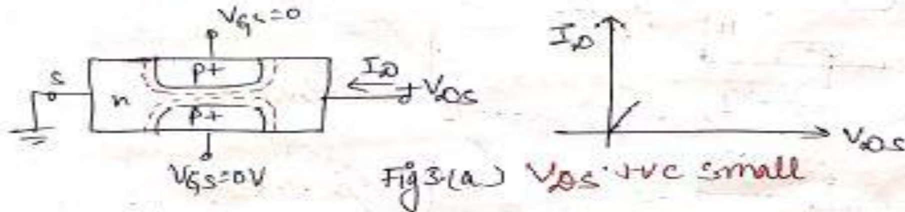


Fig 3(a) V_{DS} +ve small

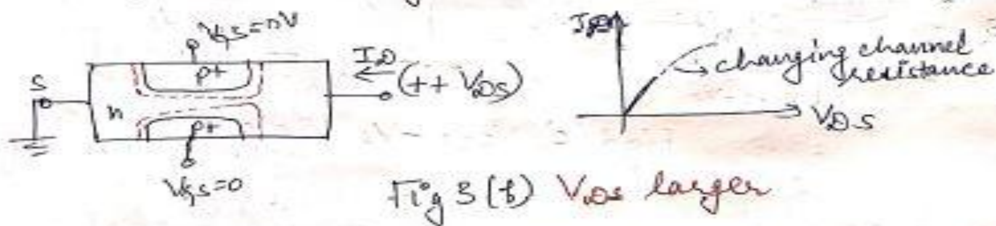


Fig 3(b) V_{DS} larger

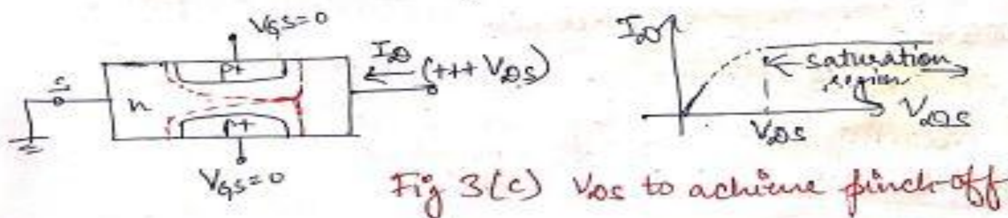


Fig 3(c) V_{DS} to achieve pinch-off

→ If drain voltage ↑ further, (fig 3(c)), channel gets pinced off. at the drain terminal.

→ Any further ↑ in V_{DS} will not increase drain current.

→ The drain voltage at pinch-off is referred as $V_{DS}(sat)$.

→ For $V_{DS} > V_{DS}(sat)$, the transistor is said to be in saturation. and I_D becomes independent of V_{DS}.

Q-3 (a) Explain the MOS structure with the aid of parallel plate capacitor. [6 Marks] CO4_L2

(b) Explain Low pressure CVD. [4 Marks] CO3_L2

Ans-3(a)

MOSFET - Two Terminal MOS structure

MOSFET - Metal Oxide Semiconductor Field Effect Transistor.

Energy Band Diagrams

→ The physics of MOS structure is explained using single parallel plate capacitor. (Fig.1)

→ Fig.2(a) shows a parallel plate capacitor with top plate at -ve voltage with respect to bottom plate

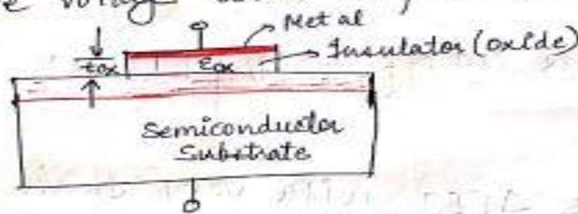


Fig 1: Basic MOS Capacitor Structure.

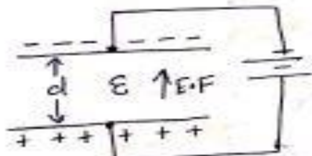


Fig 2 (a): Parallel Plate Capacitor showing E.F and conductor charges

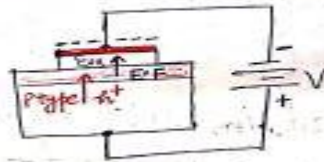


Fig2(b) MOS Capacitor with -ve gate bias.

Fig2(c) MOS Capacitor with an accumulation layer of holes.

→ An insulator material separates the two plates.

→ With this bias, -ve charge exists on the top plate and a +ve charge exists on bottom plate, and an E.F is induced between the two plates.

capacitance per unit area for this geometry is

$$C' = \frac{\varepsilon}{d} \quad \text{—(1)}$$

ε = Permittivity of insulator
d = distance between two plates

→ charge per unit area on either plate is

$$Q' = C'V \quad \text{—(2)}$$

where prime shows charge or capacitance per unit area.

→ E.F is $E = \frac{V}{d}$ —(3)

→ In Fig 2(b), if the E.F has to penetrate into the semiconductor, the majority carrier holes would experience a force toward the MOS interface.

→ Fig.2 (c) shows the equilibrium distribution of charge in MOS capacitor with the particular applied Voltage.

→ An accumulation layer of holes in oxide-semiconductor junction corresponds to the +ve charge on the bottom plate of MOS capacitor.

→ Fig 3(a) shows MOS capacitor with applied voltage which is reversed.

→ +ve charge exist on top metal plate and

the induced E·F is in the opposite direction.

→ If E·F penetrates the semiconductor, majority Carrier holes experiences a force away from the oxide-semiconductor interface.

→ As holes are pushed away from oxide-semiconductor interface, -ve space charge region is created because of fixed ionized acceptor atoms.

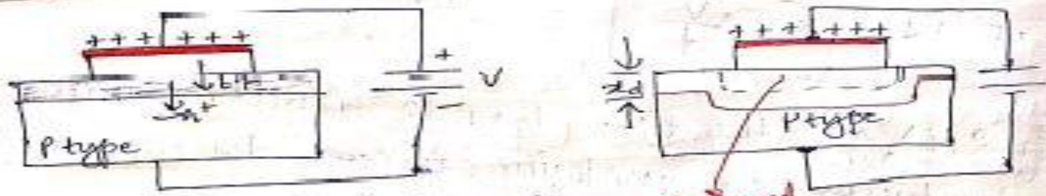


Fig 3: (a) E·F and charge flow in MOS Capacitor with +ve gate bias (b) Induced space charge region

→ Fig 4 (a) shows energy band diagram of MOS capacitor with p-type substrate, for the case when -ve voltage is applied to the top metal gate.

→ The valence edge is closer to the fermi level at the oxide - semiconductor interface than in bulk material showing the accumulation of holes.

→ The fermi level is constant in semiconductor since MOS is in thermal equilibrium and no current through oxide.

→ Fig 4 (b) shows the band diagram when +ve voltage is applied to the gate.

→ The conduction band and intrinsic fermi level move closer to the fermi level.

→ The induced space charge width is x_d.

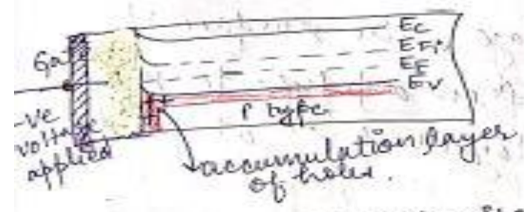


Fig 4 (a) MOS capacitor energy band diagram with -ve gate bias.

Fig 4(b) MOS capacitor energy band diagram with moderate +ve gate bias

→ Consider a still larger +ve voltage applied to top of metal gate of MOS.

⇒ It causes more E.F and more +ve and -ve charge on MOS.

→ A larger -ve charge means larger induced space charge region and more band bending. (Fig.5)

→ Fig 5, the intrinsic fermi level is now below the fermi level, thus CB is closer to fermi level than V.B is.

→ This shows that the surface in semiconductor adjacent to oxide semiconductor interface is n type.

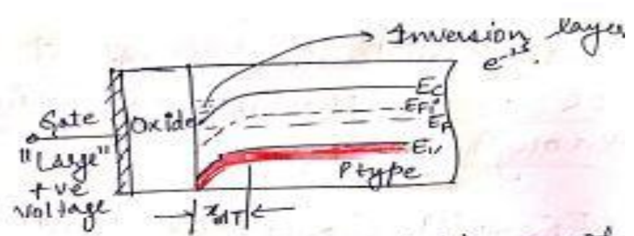
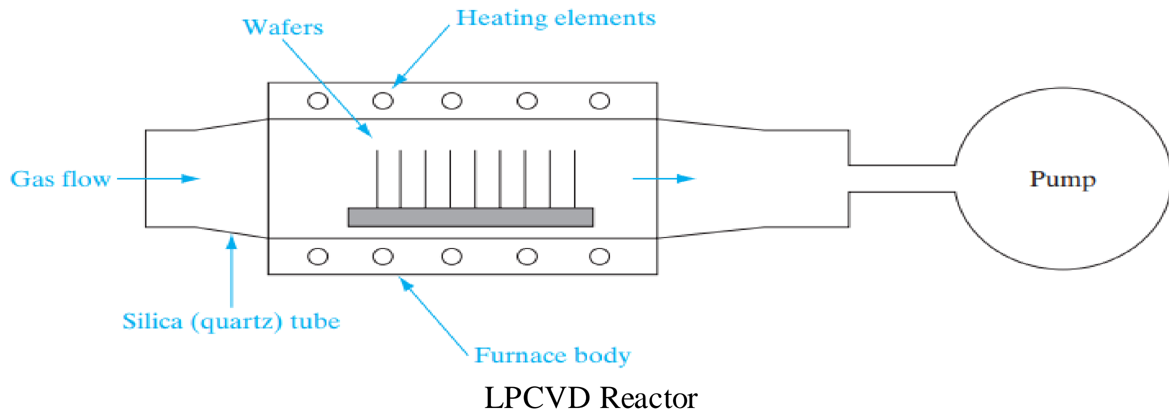


Fig 5: Energy band diagram of MOS with p-type substrate for "large" +ve gate bias.

... surface of

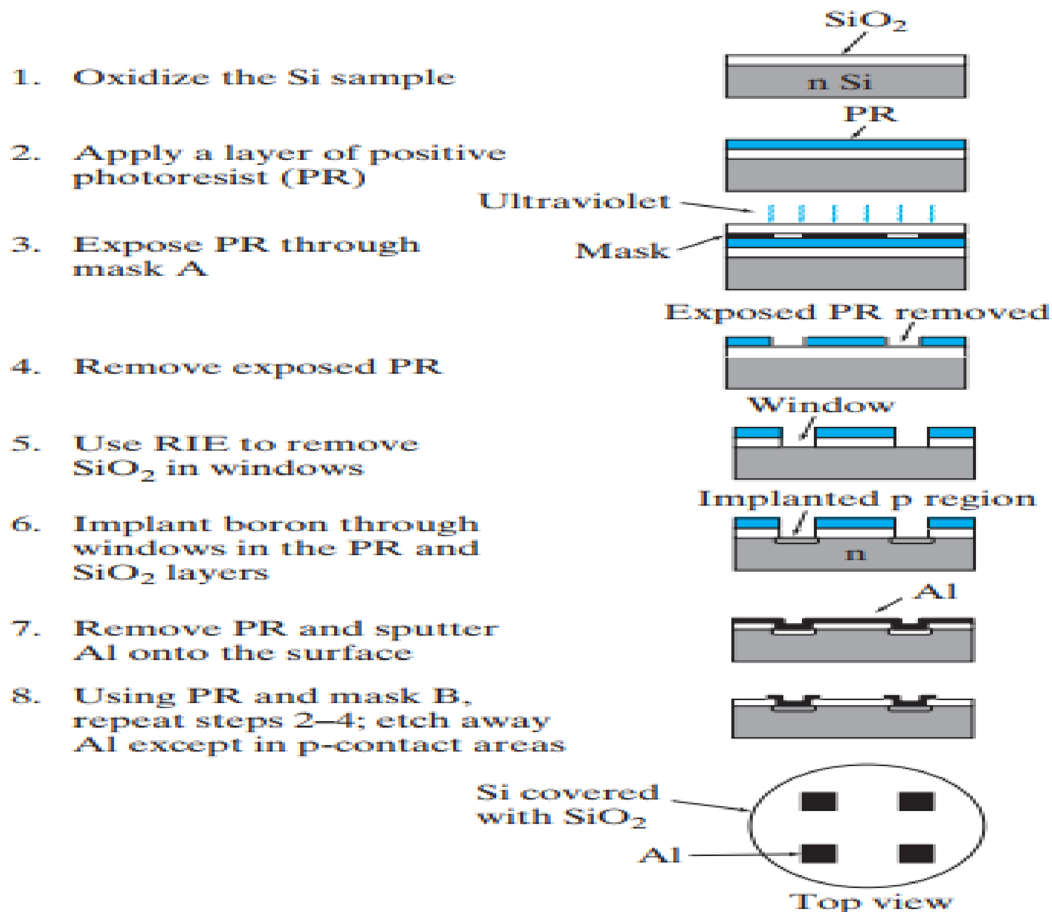
(b) ***SiO2*** films can also be formed by ***low pressure (~100 mTorr)***2 chemical vapor deposition (LPCVD) or plasma enhanced CVD (PECVD).

The key differences are that thermal oxidation consumes Si from the substrate, and very high temperatures are required, whereas CVD of ***SiO2*** does not consume Si from the substrate and can be done at much lower temperatures.
The CVD process reacts a Si-containing gas such as ***SiH4*** with an oxygen-containing precursor, causing a chemical reaction, leading to the deposition of SiO2 on the substrate.
LPCVD is also widely used to deposit other dielectrics such as ***silicon nitride (Si3N4), and polycrystalline or amorphous Si.***



LPCVD Reactor

Q-4 Explain PN Junction fabrication process in detail with relevant diagrams. [10 Marks]
CO3_L2
Ans.4



Q-5 Explain the working and I-V Characteristics of n channel enhancement type MOSFET with its circuit symbols. [10 Marks] CO4_L2

Ans-5

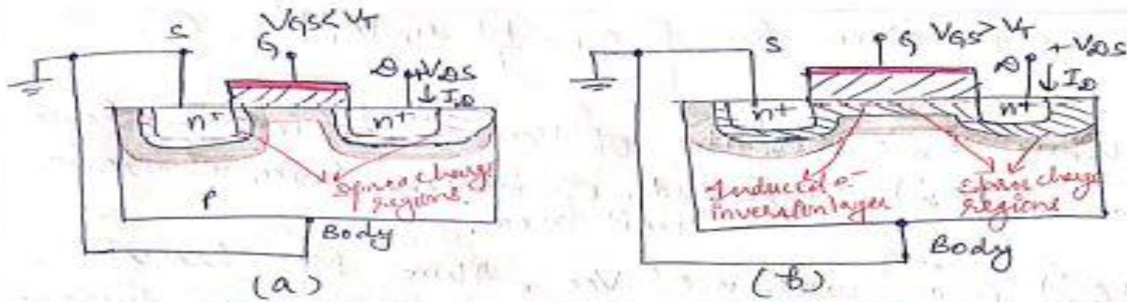


Fig 1: n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ (b) with an gate voltage $V_{GS} > V_T$.

→ Source and body are grounded.

→ With this bias configuration, there is no electron inversion layer. drain to substrate is reverse biased and drain current is zero. ($I_D = 0$).

→ Fig. 1 (b) shows the same MOSFET with $V_{GS} > V_T$.

→ An $\bar{e}$ inversion layer is created, so, that when a small V_{DS} is applied the $\bar{e}$'s in the inversion layer flows from source to +ve drain terminal.

→ There is no current through the oxide to the gate terminal.

→ For small V_{DS}, the channel regions has characteristics of resistor, so,

$$I_D = g_d V_{DS} \quad (1)$$

g_d is channel conductance in the limit as $V_{DS} \to 0$.

→ g_d is given by $g_d = \frac{W}{L} \mu_n |Q_n'|$ — (2)

where μ_n = mobility of the $\bar{e}$'s in inversion layer
$|Q_n'|$ = magnitude of inversion layer charge per unit area.

→ $|Q_n'|$ is a function of V_{GS}, thus MOS transistor action is the modulation of channel conductance by gate voltage.

→ channel conductance in turn determines I_D.

→ Fig. 2 shows I_D vs V_{DS} curve for small V_{DS}.

→ When $V_{GS} < V_T$, the $I_D = 0$.

→ As V_{GS} becomes greater than V_T, the channel inversion charge density increases, ⇒ increases the channel conductance.

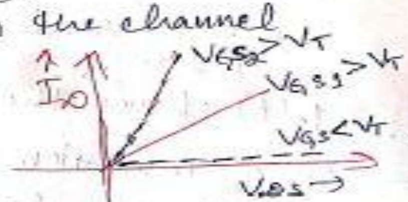


Fig2: I_D vs V_{DS} curve for small V_{DS} at three V_{GS} voltages.

→ Fig. 3(a) shows, basic MOS structure for the case $V_{GS} > V_T$ and applied small V_{DS}.

→ The thickness of the inversion layer shows the relative charge density.

→ Fig 3(b) shows, case for ~~V_{DS} value~~ increase V_{DS}.

→ As drain voltage increases, the voltage drop across the oxide near drain terminal decreases.

→ this implies that the induced inversion charge density near the drain also ↓.

→ Incremental conductance of channel at drain ↓ meaning that slope of I_D vs V_{DS} ↓.

→ When V_{DS} increases to the point where the potential drop across the oxide at the drain is equal to V_T, the induced inversion charge density is zero at the drain terminal. (as shown in fig. 3(c)).

→ At this point incremental conductance at drain is zero, meaning that slope of I_D vs V_{DS} = 0.

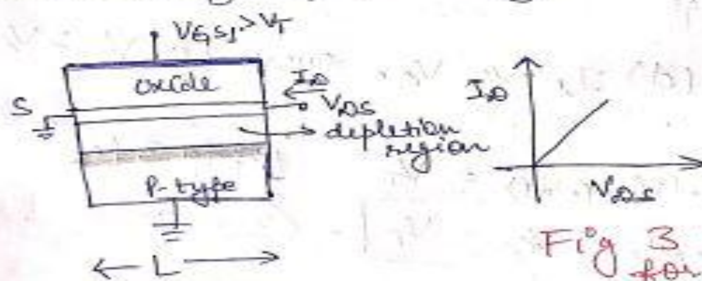


Fig 3 (a) I_D vs V_{DS} curve for a ~~large~~ small V_{DS}

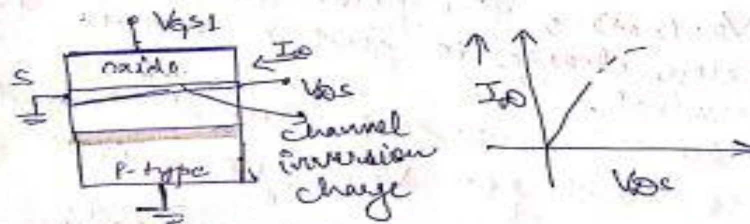
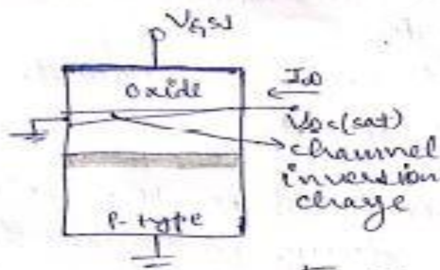


Fig 3 (b) I_D vs V_{DS} curve for larger V_{DS} value;



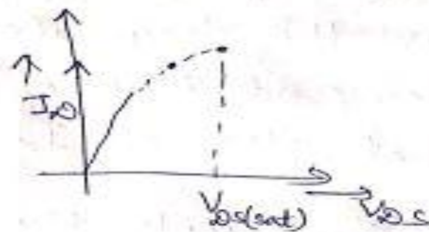
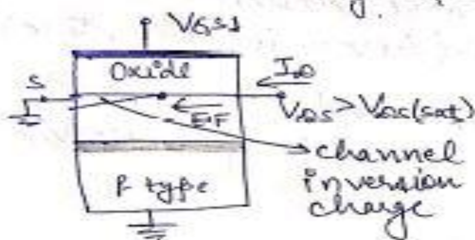


Fig 3 (c) I_D vs V_{DS} curve for $V_{DS} = V_{DS(sat)}$



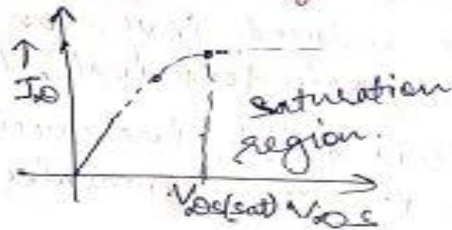


Fig 3 (d) I_D vs V_{DS} curve for $V_{DS} > V_{DS(sat)}$

We have, $V_{GS} - V_{DS(sat)} = V_T$ [fig 3(c)]

$$\Rightarrow \boxed{V_{DS(sat)} = V_{GS} - V_T} \quad — (3)$$

→ When $V_{DS} > V_{DS(sat)}$, the point in the channel at which inversion charge is just 0 moves towards the source terminal.

→ If ΔL (channel length) now < L (original channel length) I_D will be constant for $V_{DS} > V_{DS(sat)}$.

→ I_D vs V_{DS} characteristics shows saturation region (fig 3(d)).

→ Fig. 4 shows I_D vs V_{DS} curves for n-channel enhancement mode MOSFET.

→ If V_{GS} ↑, initial slope of I_D vs V_{DS} ↑.

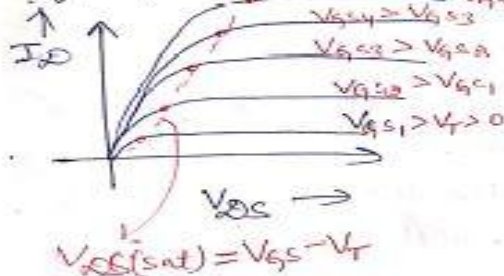


Fig. 4: I_D vs V_{DS}
n-channel enhancement mode MOSFET

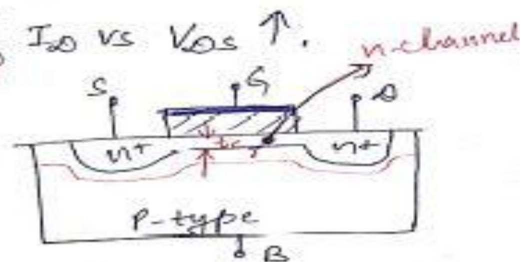


Fig. 5 n-channel depletion MOSFET.