Date:
16.12.20

IAT - 3

TCE, SEM 7, VLSI

Q)1 Obtain scaling factor for following device parameters:

(i) Gate area

$$A_g = L \cdot W$$

where, L = channel length and W = channel width

Both are scaled by $1/\alpha$

Thus, A_g is scaled by $(1/\alpha)^2$

(ii) Gate capacitance per unit area

$$C_o = \frac{\epsilon_{ox}}{D}$$

where,

ϵ_{ox} = permittivity of gate oxide (thinox)

and D = gate oxide thickness scaled by $(1/\beta)$

Thus, C_o is scaled by $1/1/\beta = \beta$

(iii) Gate capacitance

$$C_g = C_o L W$$

Thus, C_g is scaled by $\beta\left(\frac{1}{\alpha^2}\right) = \beta/\alpha^2$

(iv) Parasitic Capacitance

C_x is proportional to A_x/d

where, A_x = area of depletion region around source or drain scaled by $(1/\alpha^2)$

and d = depletion width around source or drain which is scaled by $(1/\alpha)$

Thus, C_x is scaled by $(1/\alpha^2) \cdot 1/1/\alpha = 1/\alpha$

(v) Carrier density in channel

$$Q_{ON} = C_o \cdot V_{gs}$$

where, Q_{ON} = average charge per unit area in the channel in 'ON' state

C_o is scaled by β ⇒ Thus, Q_{ON} is scaled by

V_{gs} is scaled by $1/\beta$ $\beta(1/\beta) = 1$

Q)3 Discuss the design of 4 bit adder.

Ans:

Inputs			Outputs	
A_K	B_K	C_{K-1}	S_K	C_K
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

where, A_K and B_K are two inputs

C_{K-1} = previous carry

S_K = sum and C_K = new carry

For any column k, there will be three inputs which are corresponding bits of input numbers A_K and B_K and carry in C_{K-1} and two outputs sum and carry out.

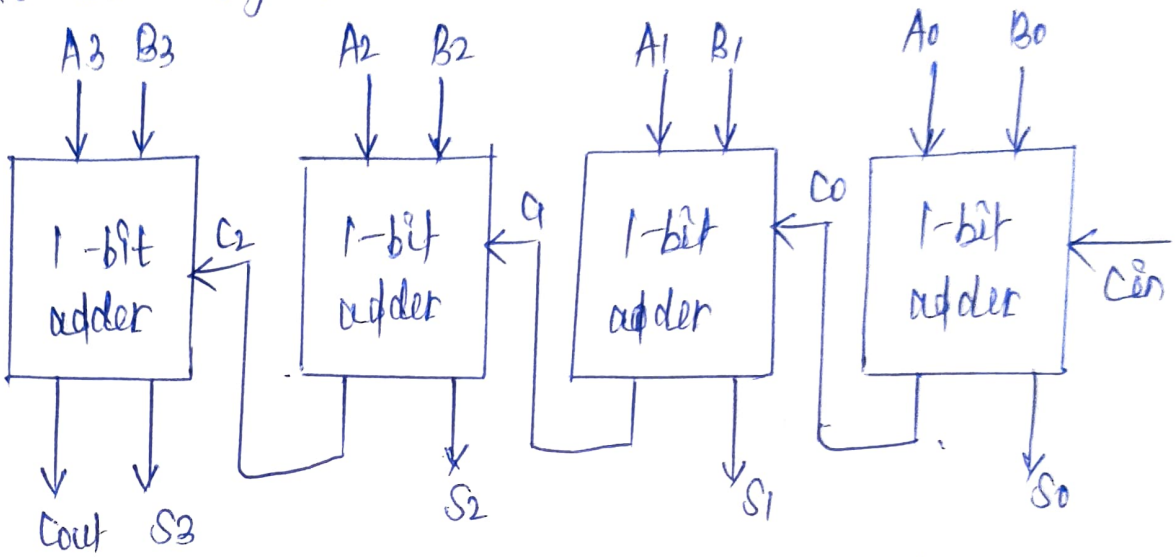
where, Sum, $S_K = H_K \overline{C_{K-1}} + \overline{H_K} C_{K-1}$

Carry out, $C_K = A_K B_K + H_K C_{K-1}$

where H_K = half sum where, $0 \le K \le n-1$ for n-bit numbers

$H_K = \overline{A_K} B_K + A_K \overline{B_K}$

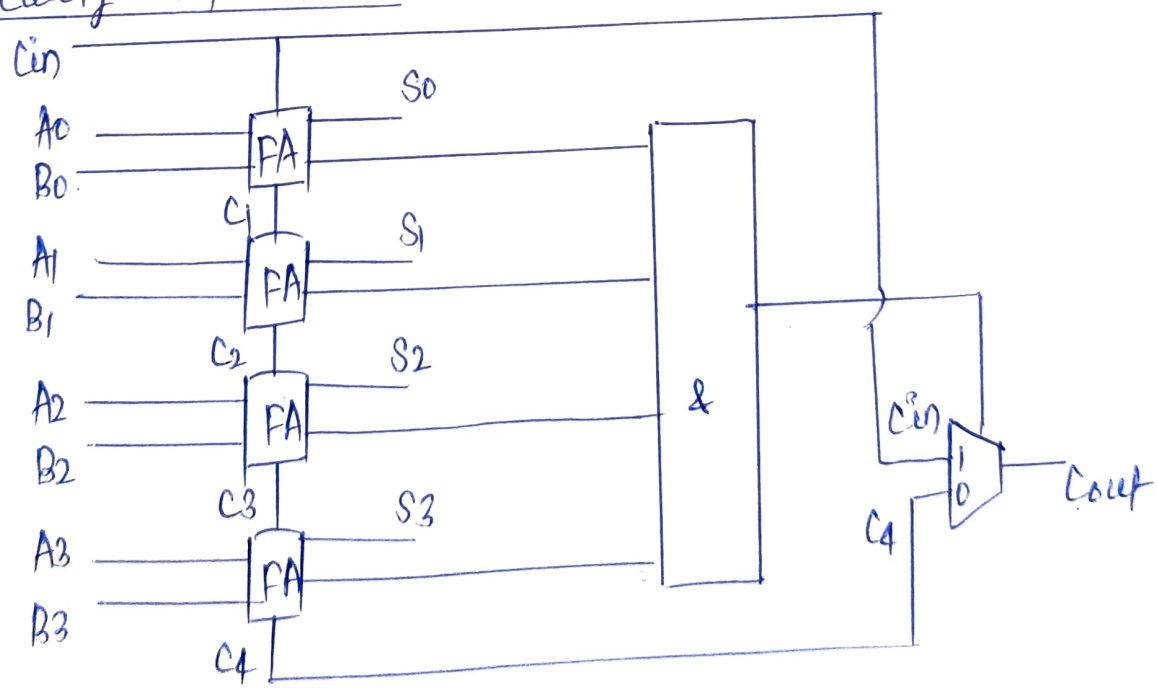
In order to form 4 bit adder, 4 adder elements must be cascaded with Ck of previous element connecting to carry in of next more significant element.



$A_0 - A_3$ = input A (4 bits), Cin = carry input (1-bit)
$B_0 - B_3$ = input B (4 bits), $S_0 - S_3$ = sum (4 bits)
Cout = carry out (1 bit)

Q.4 Write notes with relevant diagrams and equations on:

1) Carry skip adders



Carry skip adder "skips" the internal carry bits and improves on the delay of ripple carry adder.

It is also known as by pass adder.
All the sum outputs are computed by corresponding full adders. Another output is computed that is named as propagate signal.

$$P = A \oplus B$$

∴ P_0, P_1, P_2 and P_3 are computed.
All these are "anded" together and their output becomes select line that selects "Cin" or the "C4" of n^{th} full adder as final carry out of the system.
Total worst case propagation delay time, T

$$T = 2(P-1)k_1 + (M-2)k_2$$

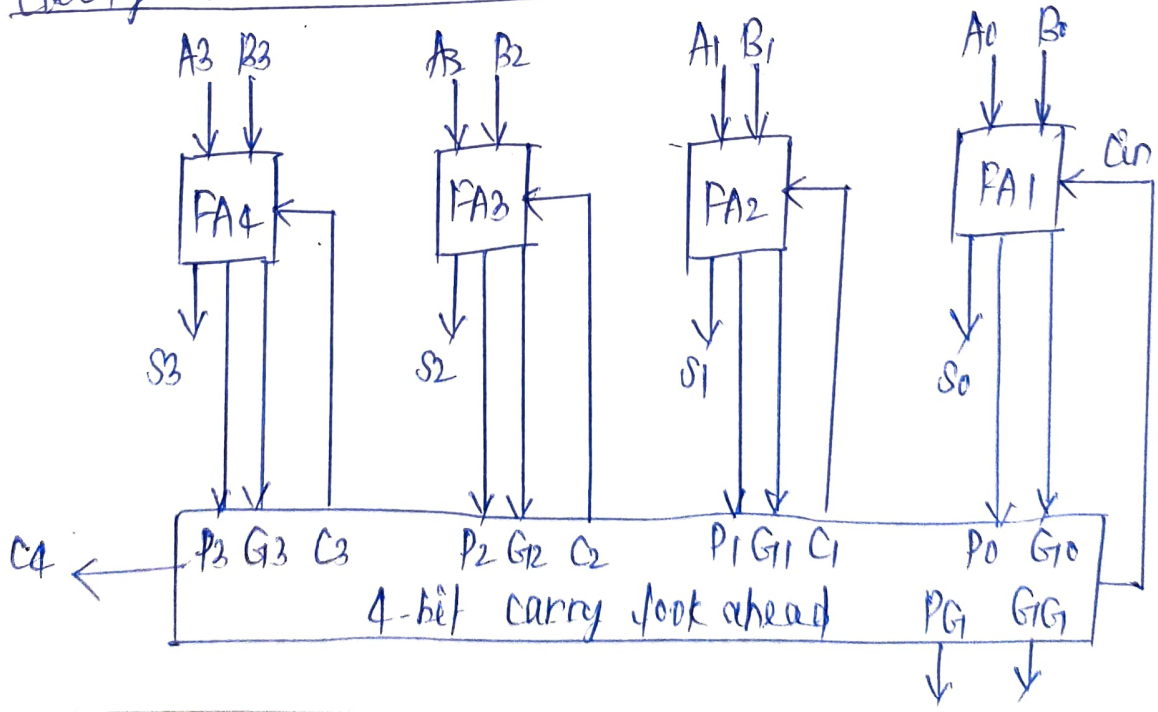
$P = n/M$ Min value of T is reached when

$$M = \sqrt{2n \cdot k_1/k_2}$$

where, k_1 = time needed for carry signal to propagate through adder cell

k_2 = time needed for carry to skip over a block

(iii) Carry look ahead adder



Carry look ahead adder are fastest adder. because the computation is reduced. The carry bit of block FA_2 don't depend on previous block. The carry in bit of FA_2 is computed on basis of P_0 and G_0 signals, i.e; propagate and generate signals. Since, carry bits are not cascaded, rippling effect causing delay in ripple carry adders is completely removed. Therefore, these are best in order to reduce delay.

Now, P_i = carry propagate and G_i = carry generate

$$p_i = A_i \oplus B_i, \quad G_i = A_i B_i$$

$$\therefore S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_i C_i$$

Where, G_i produces carry when both A_i and B_i are 1 regardless of input carry.

P_i is associated with propagation of carry from C_i to C_{i+1}.

$$\therefore C_4 = G_0 + P_0 C_{in}$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{in}$$

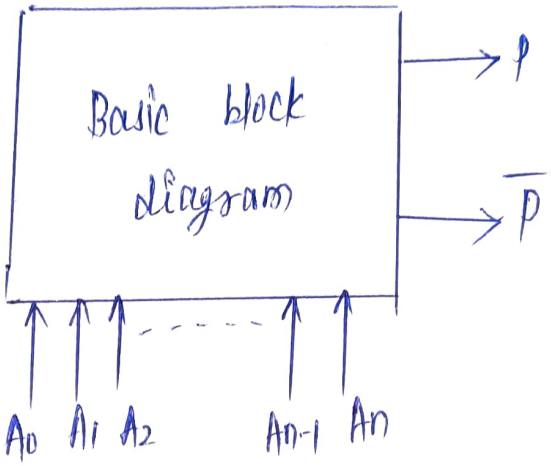
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 G_2 G_1 + P_3 P_2 P_1 G_0 + P_1 P_3 P_2 P_0 C_{in}$$

From these four equations, it can be observed that C_4 doesn't have to wait for C_3 and C_2 to propagate at same time as C_3 and C_2

Q)5 Explain structured design approach for implementation of parity generator with relevant stick diagram.

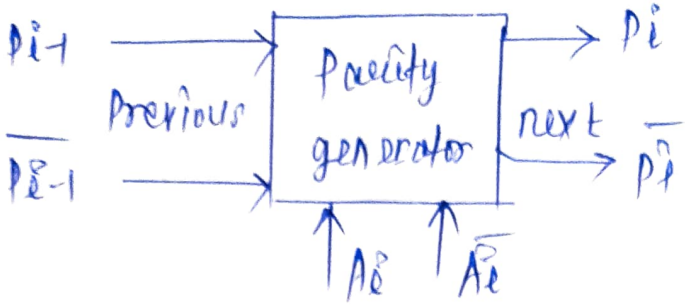
Ans: Parity generator consists of certain number of inputs. It the number of 1's is odd then output P is 1 else 0. This block contains (n+1) no. of cells with each cell having two bit input in addition with previous parity bit. However, for first cell, initial parity bit is zero.

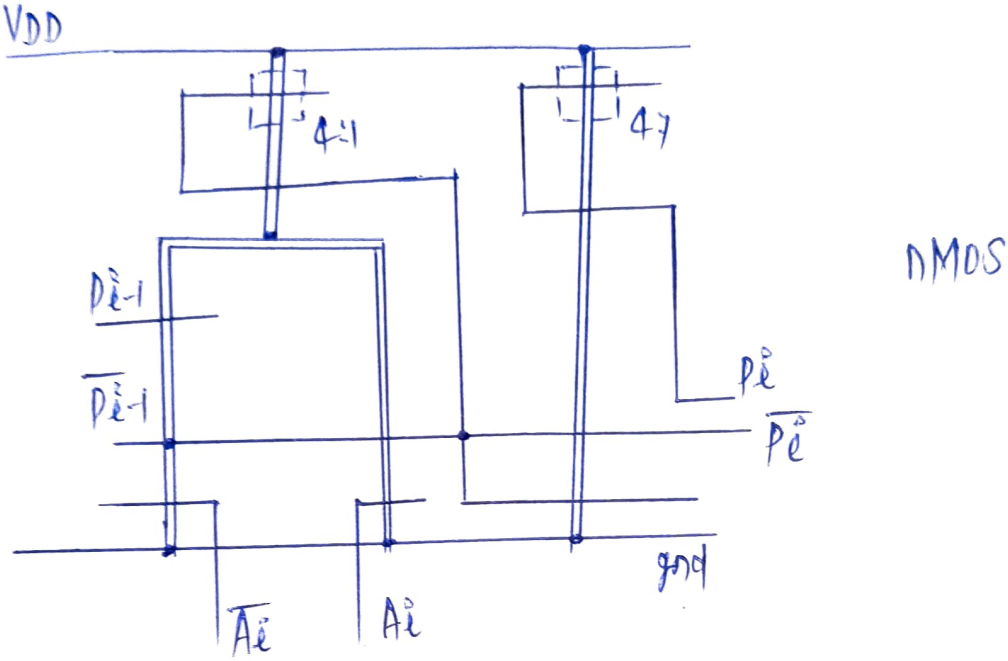


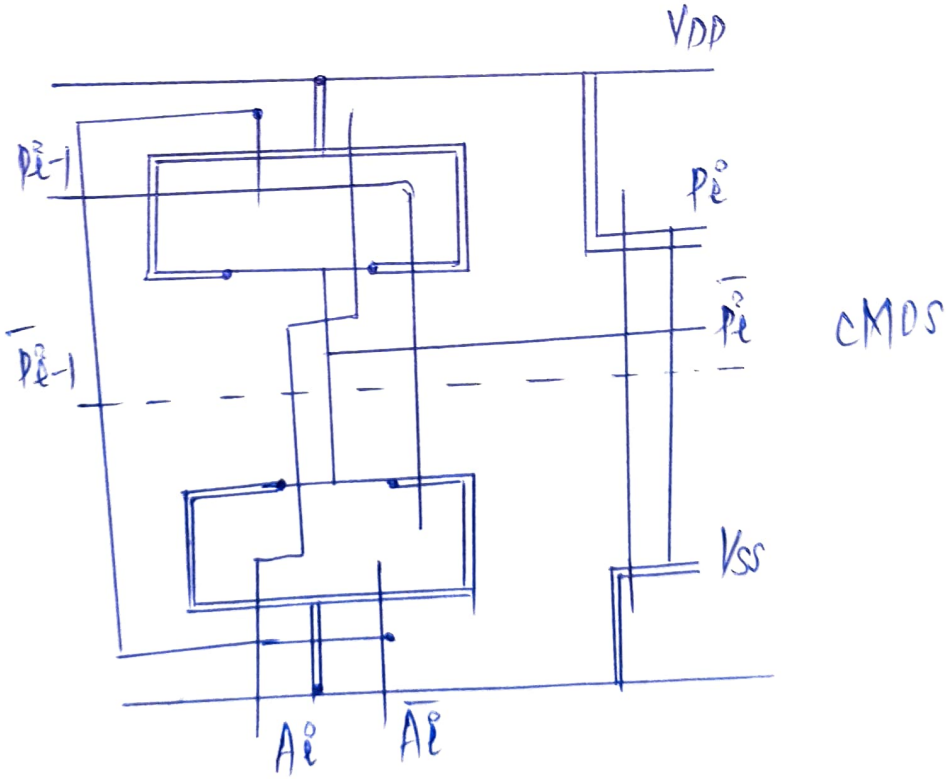
One bit parity cell

Stage of previous stage parity signal	Present stage binary input	Present stage parity signal
P_{i-1}	A_i	P_i
0	0	0
0	1	1
1	0	1
1	1	0

- no. of 1's odd in previous stage then output P_{i-1} is 1 else 0.

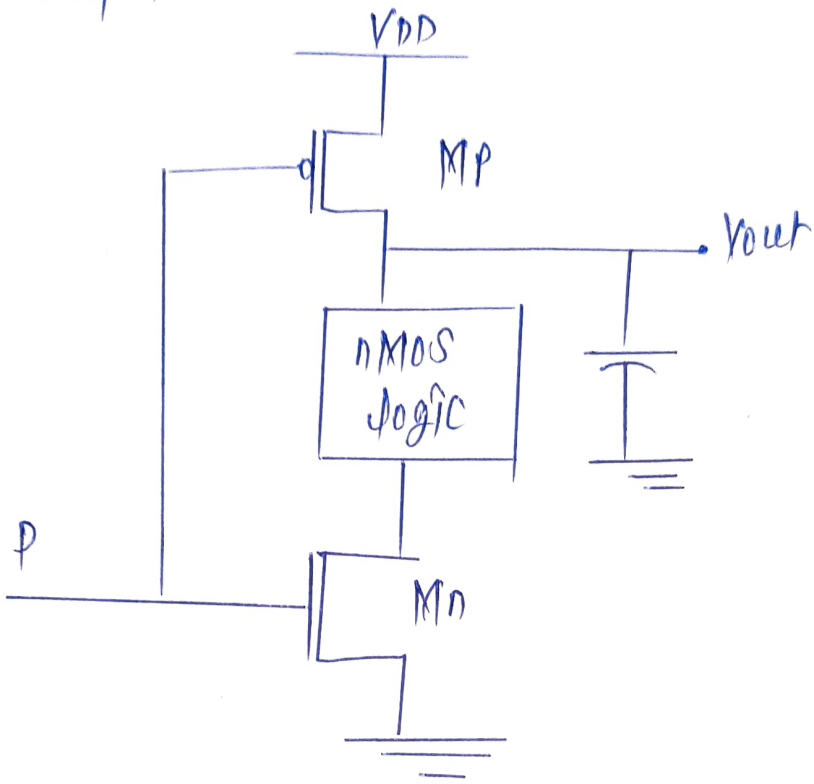






Q6 Explain dynamic CMOS and domino CMOS logic.

Ans: A dynamic CMOS logic users charge storage and clocking properties of MOS transistor. Hence the clock drives nMOS evaluation transistor and pMOS precharge transistor. A logic is implemented using an nFET array connected between output node and ground.



CMOS domino logic

Domino CMOS logic is modified version of dynamic CMOS logic circuit. In this, a static inverter is connected at the output of each dynamic CMOS logic block. The addition of inverter solves the problem of cascading of dynamic CMOS logic circuits.