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10ES33

Third Semester B.E. Degree Examination, June/July 2017
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the following (i) POS (ii) Truth table (iii) Karnaugh map. **(06 Marks)**

b. Find the minimal SOP of,

(i) $f(w,x,y,z) = \sum m(0,1,2,3,4,9,13) + dc(5,10,11,14)$

(ii) $f(w,x,y,z) = \pi M(0,3,4,11,13) + dc(2,6,8,9,10)$ **(07 Marks)**

c. Find the minimal sum and minimal product of,
$f(a,b,c,d) = \pi M(0,2,6,11,13,15) + dc(1,9,10,14)$ **(07 Marks)**

2 a. Obtain SOP using Quine-Mc Clusky method of,
$f(w,x,y,z) = \sum m(7,9,12,13,14,15) + dc(4,11)$ **(12 Marks)**

b. Simplify the function using VEM technique by considering a, b and c are map variables,
$f(a,b,c,d) = \sum m(2,3,4,10,13,14,15) + dc(7,9,11)$ **(08 Marks)**

3 a. Using AND decoder realize full adder with its truth table, output function and decoder of suitable type. **(06 Marks)**

b. Design 8 : 3 higher order priority encoder. Mention its advantage. **(08 Marks)**

c. Construct 16 : 1 MUX using 4 : 1 MUX. **(06 Marks)**

4 a. Design 2 bit magnitude comparator with its truth table, simplified output equations and logic circuit. **(10 Marks)**

b. Realize and implement using 8 : 1 MUX where w, x, y appear as S_2,S_1 and S_0 of
$f(w,x,y,z) = \sum m(0,4,6,8,9,11,13,14)$
Also realize by 4 : 1 MUX where w, x appears as S_1, S_0. **(10 Marks)**

PART – B

5 a. Briefly explain sequential logic circuit. Explain TFF and JK Master Slave FF with their logic symbol, truth table, logic diagram and timing diagram. **(10 Marks)**

b. Explain race around condition and how it is over come. **(04 Marks)**

c. Explain the working of a SR latch as a switch debouncer with necessary circuit and timing diagram. **(06 Marks)**

6 a. Derive the characteristics equation of JK-FF and D-FF. **(06 Marks)**

b. With a neat diagram of 4-bit Universal Shift Register (USB) explain its working with the help of mode table. **(08 Marks)**

c. Design mod-10 asynchronous counter using clocked T-FFs. **(06 Marks)**

7 a. Explain 4-bit ring counter with a neat diagram. **(06 Marks)**

b. Explain the triggering of flipflops and its types. **(04 Marks)**

c. Design and implement a synchronous counter for the sequence 2 – 0 – 7 – 4 – 1 using negative edge clocked JK flip flop. **(10 Marks)**

8 a. Bring out the differences between Mealy and Moore machine models. **(08 Marks)**

b. Construct the excitation table, transition table, state table and state diagram for Moore circuit shown in Fig. Q8 (b). **(12 Marks)**

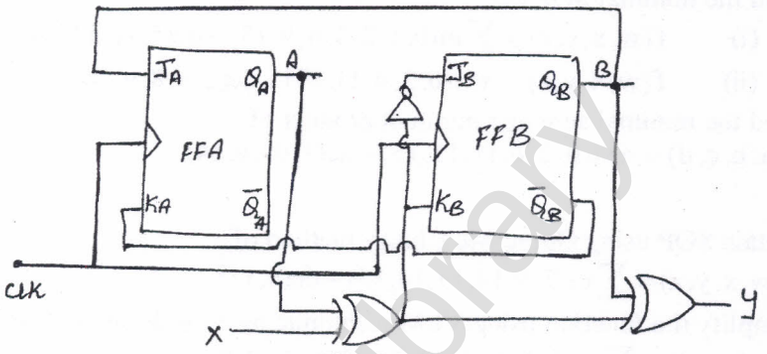

Fig. Q8 (b)

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