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10ES32

Third Semester B.E. Degree Examination, June/July 2017
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With respect to a semiconductor diode, explain the following:
(i) Reverse recovery time
(ii) Diffusion capacitance. **(06 Marks)**

b. Explain the working of full wave bridge rectifier and derive the expression for ripple factor and efficiency. **(08 Marks)**

c. Design an ideal clamper circuit to obtain the output waveform as shown in Fig. Q1 (c) for the given input. **(06 Marks)**

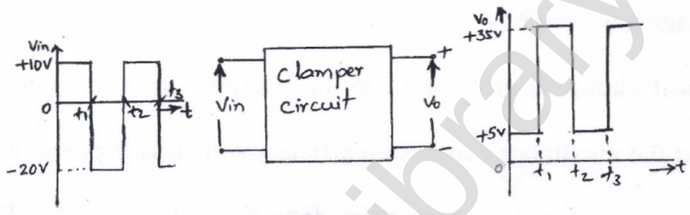

Fig. Q1 (c)

2 a. Explain with help of load line the effect of variation of V_{CC}, I_B on Q-point of a transistor. **(06 Marks)**

b. Derive the expression for stability factors for voltage divider bias circuit with respect to I_{CO}, V_{BE} and β. **(06 Marks)**

c. Determine the voltage V_{CE} and the current I_C for the voltage divider configuration shown in Fig. Q2 (c) **(08 Marks)**

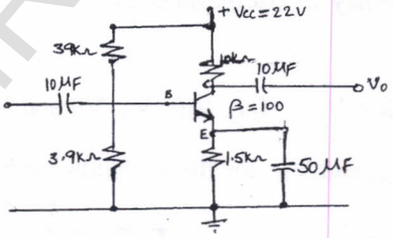

Fig. Q2 (c)

3 a. Draw the re-equivalent circuit of CE fixed bias configuration and derive the expression for Z_{in}, Z_O and A_V. **(10 Marks)**

b. What are the advantages of h-parameters? **(04 Marks)**

c. For the network shown in Fig. Q3 (c), determine r_e, Z_i, Z_o, A_v. **(06 Marks)**

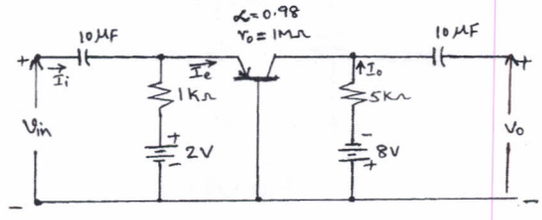

Fig. Q3 (c)

4 a. Obtain expression for Miller effect input and Miller effect output capacitance. **(06 Marks)**

b. Draw and discuss the effect of various capacitors on high frequency response. **(06 Marks)**

c. Determine the lower cutoff frequency for the voltage divider bias BJT amplifier with $C_S = 10\,\mu F, C_C = 1\,\mu F, C_E = 20\ \mu F$, $R_S = 1\ K\Omega$, $R_1 = 40\,K\Omega$, $R_2 = 10\,K\Omega$, $R_E = 2\ K\Omega$, $R_C = 4\ K\Omega$, $R_L = 2.2\ K\Omega$, $\beta = 100$, $r_0 = \infty\ \Omega$, $V_{CC} = 20V$ **(08 Marks)**

PART – B

5 a. Explain the important advantages of a negative feedback amplifier. **(04 Marks)**

b. Obtain expression for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

c. Why do we cascade amplifier? State the various method of cascading transistor amplifier. A given amplifier arrangements has the following voltage gains. $A_{V_1} = 10$, $A_{V_2} = 20$ and $A_{V_3} = 40$. What is the overall voltage gain? Also express each gain in dB and determine the total voltage gain in dB? **(08 Marks)**

6 a. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier. **(06 Marks)**

b. Prove that the maximum conversion efficiency in class B power amplifier is 78.5%. **(08 Marks)**

c. A power amplifier has harmonic distortions $D_2 = 0.1$, $D_3 = 0.02$, $D_4 = 0.01$, the fundamental current $I_1 = 4$ Amps and $R_L = 8\ \Omega$. Calculate the total harmonic distortion, fundamental power and total power. **(06 Marks)**

7 a. State Barkhausen criteria for sustained oscillations apply this to a transistorized Weinbridge oscillator and explain its operation. **(10 Marks)**

b. Explain the working of BJT Colpitt's oscillator. **(06 Marks)**

c. Calculate the frequency of oscillations of a Colpitt's oscillator, L = 100 μH, $C_1 = 100$ pF, $C_2 = 1000$ pF. **(04 Marks)**

8 a. Derive expression for V_{GSQ}, I_{DQ}, V_{DS}, V_S, V_G and V_D for a self bias JFET circuit. **(10 Marks)**

b. Determine I_{DQ}, V_{GSQ} and V_{DS} for the P-channel JFET of Fig. Q8 (b). **(10 Marks)**

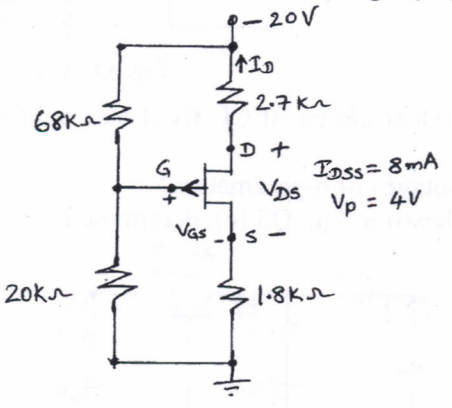

Fig. Q8 (b)

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