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10CS74

Seventh Semester B.E. Degree Examination, June/July 2017
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define the following terms : i) Computer Architecture ii) Learning curve iii) Response time iv) Throughput. **(04 Marks)**

b. Define Amdahl's law. Derive an expression for CPU clock as a function of instruction count, clock per instruction and clock cycle time. **(08 Marks)**

c. Find the die yield for dies that are 1.5cm on a side and 1.0cm on a side, assuming a defect density of 0.4 per cm^2 and is 4. **(04 Marks)**

d. Explain the main measures of dependability. **(04 Marks)**

2 a. What is Pipeline? Explain the basic of RISC instruction set. **(06 Marks)**

b. What are the major hurdles of pipeling? Illustrate the data hazard. **(10 Marks)**

c. Consider the unpipelined processor in RISC. Assume that it has a 1ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline? **(04 Marks)**

3 a. Explain how Tomasulo's algorithm can be extended to support speculation. **(08 Marks)**

b. What are the basic compiler techniques for exposing ILP? Explain briefly. **(08 Marks)**

c. Explain the dynamic branch prediction state diagram. **(04 Marks)**

4 a. What are the types of dependencies? Explain in detail with example. **(10 Marks)**

b. Explain the seven fields of each reservation station and register field. **(06 Marks)**

c. Suppose we have a VLIW that could issue two memory references, two FP operations and one integer operations or branch in every clock cycle, show an unrolled version of the loop x(i) = x(i) + S, for such a processor. Unroll as many times as necessary to eliminate any stalls. Ignore the delayed branches : **(04 Marks)**

MIPS	Code
Loop : L.D	F_0, O(R1) ;
ADD.D	F_4, F_0, R_2 ;
S.D	F_4, O(R1) ;
DADDU1	R1, R1 , # -8 ;
BNE	R1, R2, LOOP ;

PART – B

5 a. With a neat diagram, explain the basic structure of a centralized shared memory and distributed memory multiprocessor. **(08 Marks)**

b. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential? **(04 Marks)**

c. Explain basic schemes for enforcing coherence. **(08 Marks)**

6 a. Explain the six basic cache optimization techniques. **(10 Marks)**

b. With a neat diagram, explain the hypothetical memory hierarchy. **(10 Marks)**

7 a. Explain the following advanced optimization of cache :

i) Compiler optimizations to reduce miss rate.

ii) Merging write buffer to reduce miss penalty.

iii) Critical word first and early restart to reduce miss penalty. **(09 Marks)**

b. Assume that the hit time of a two way set associative first level data cache is 1.1 times faster than a four – way set – associative cache of the same size. The miss falls from 0.049 to 0.044 for an 8kB data cache. Assume a hit is 1clock cycle and that the cache is the critical path for the clock. Assume that the miss penalty is 10 clock cycles to the L2 cache for the two way set associative cache and that the L2 cache does not miss, which has the faster average memory access time? **(06 Marks)**

c. Explain Internal organization of 64Mb DRAM. **(05 Marks)**

8 a. Explain in detail the hardware support for preserving exception behaviour during speculation. **(10 Marks)**

b. Explain hardware support for exposing parallelism for VLIW & EPIC. **(10 Marks)**

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