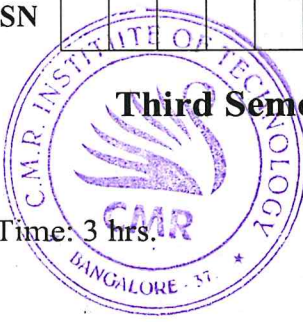


CBCS SCHEME

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17EE34



Third Semester B.E. Degree Examination, July/August 2021 Analog Electronic Circuits

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- 1 a. Define clipping circuit, for the circuit shown in Fig.Q.1(a) determine the output for the given input. Assume silicon diode. (08 Marks)

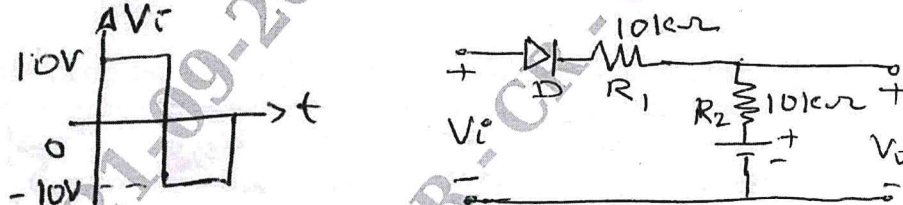


Fig.Q.1(a)

- b. Explain with the help of a neat diagram the operation of double ended (Two way) clipping circuit with-different bias voltages. (06 Marks)
- c. For the circuit shown in Fig.Q.1(c) determine I_B , I_C , V_{CE} , V_B , V_C and V_E . (06 Marks)

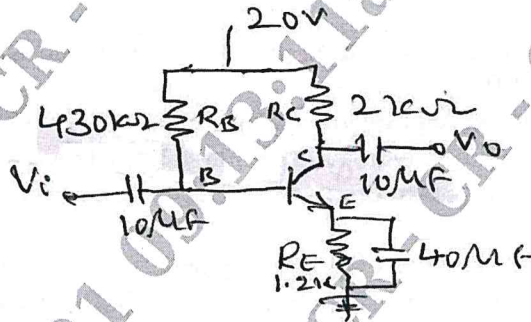


Fig.Q.1(c)

- 2 a. For the fixed bias transistor circuit derive expression for stability factor S_{ICO} , $S_{V_{BE}}$ and S_{β} . Draw the circuit diagram. (10 Marks)
- b. For the voltage divider circuit shown in Fig.Q.2(b) determine R_1 , I_C , V_B , V_E and S_{ICO} . (10 Marks)

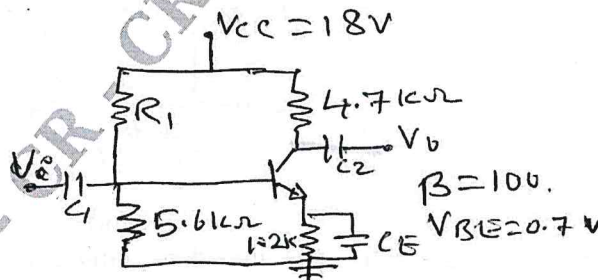
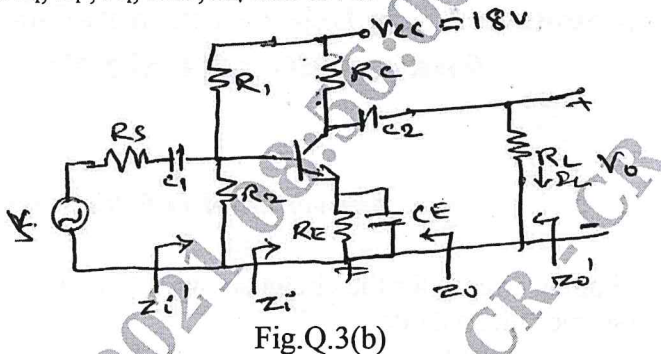


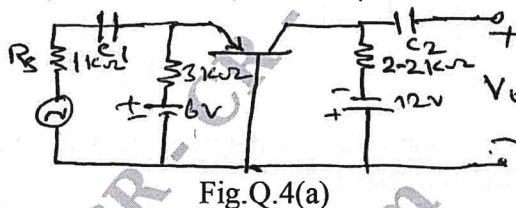
Fig.Q.2(b)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

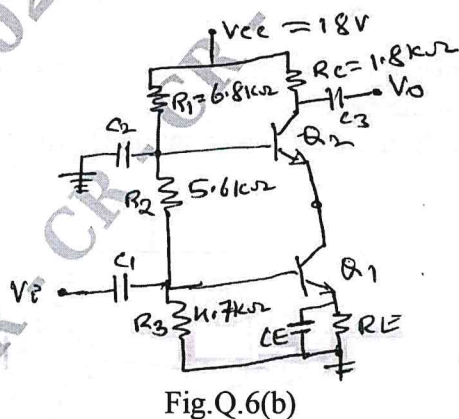
- 3 a. Define h-parameters. Derive h-parameter model for transistor and draw the h-parameter equivalent circuit for common emitter configuration. (10 Marks)
- b. For the common emitter amplifier shown in Fig.Q.3(b) with $R_S = 1K\Omega$, $R_1 = 50K\Omega$, $R_2 = 2K\Omega$, $R_C = 1K$, $R_L = 1.2K$, $h_{fe} = 50$, $h_{ie} = 1.1K\Omega$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$. Find Z_i , Z_i' , A_i , A_{IS} , A_v and A_{VS} . (10 Marks)



- 4 a. For the common base amplifier shown in Fig.Q.4(a) determine Input Impedance, current gain, voltage gain and output Impedance using complete hybrid equivalent model. Take $h_{ie} = 1.6K\Omega$, $h_{fe} = 110$, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 20\mu s$. (10 Marks)



- b. State and prove Millers theorem. (10 Marks)
- 5 a. Explain the need of cascading amplifier. Draw and explain the block diagram of three stage cascade amplifier. (08 Marks)
- b. Draw the block diagram of voltage series feed back amplifier and derive expression for voltage gain input impedance and output impedance with feed back. (08 Marks)
- c. List the important characteristics of Darlington Emitter-follower. (04 Marks)
- 6 a. Discuss the advantages of employing negative feed back in amplifiers. (08 Marks)
- b. For the cascade connection shown in Fig.Q6(b). Calculate the voltages V_{B1} , V_{B2} , V_{C2} , V_{E1} and current I_{C1} and I_{C2} . (04 Marks)



- c. Determine the voltage gain, input impedance and output impedance with feed for voltage series feed back having $A = -80$, $Z_{in} = 10K\Omega$, $Z_o = 20K\Omega$ for feedback of i) $\beta = -0.2$ ii) $\beta = -0.6$. (08 Marks)

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- 7 a. Explain the operation of class A transformer coupled power amplifier and prove that the maximum efficiency is 50%. (10 Marks)
- b. Draw the circuit of Wein Bridge oscillator and derive expression for frequency of oscillations. Also show that gain of amplifier must be at least 3 for the oscillations to occur. (10 Marks)
- 8 a. Draw the circuit of complementary symmetry class B push pull amplifier and explain its operation with waveforms. (08 Marks)
- b. A Quartz crystal has $L = 0.12H$, $C = 0.04p.f.$, $C_M = 1pf$ and $R = 9.2K\Omega$. Find series resonant frequency and parallel resonant frequency. Also find Q-factor of the crystal. (06 Marks)
- c. A power amplifier has harmonic distortions $D_2 = 0.1$, $D_3 = 0.02$, $D_4 = 0.01$, the fundamental current $I_1 = 4A$ and $R_L = 8\Omega$. Calculate the total harmonic distortion, fundamental power and total power. (06 Marks)
- 9 a. With the help of neat diagrams, explain the construction, working and characteristics of n-channel JFET. (10 Marks)
- b. For the following circuit shown in Fig.Q.9(b). Find voltage gain, Input Impedance and output Impedance i) If $r_d = 20K\Omega$ ii) If $r_d = \infty$. (10 Marks)

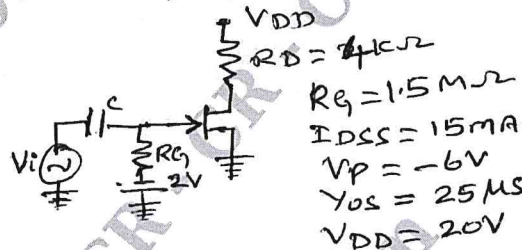


Fig.Q.9(b)

- 10 a. Explain with the help of neat diagrams, construction working, and characteristics of n-channel depletion MOSFET. (10 Marks)
- b. For the voltage divider biased n-channel JFET shown in Fig.Q.10(b). Derive expression for V_{GS} , V_{DS} , V_D and V_S . (04 Marks)

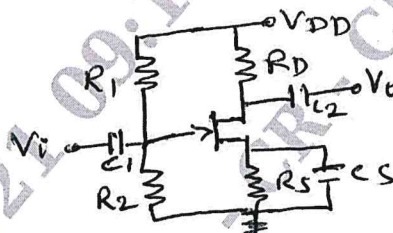


Fig.Q.10(b)

- c. For the Depletion-MOSFET amplifier shown in Fig.Q.10(c), calculate Input Impedance, output Impedance and voltage gain. (06 Marks)

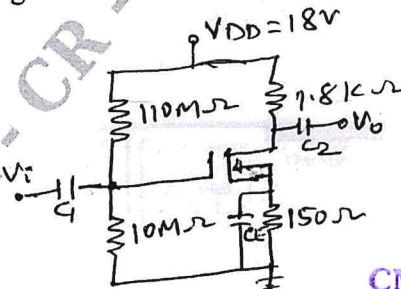


Fig.Q.10(c)

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