CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, July/August 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Define and explain combinational logic with neat figure. **(04 Marks)**

b. $y = f(A, B, C) = A + BC$. List all Min terms and Max terms. **(06 Marks)**

c. Simplify $Q = f(A, B, C, D, E) = m_0 + m_1 + m_2 + m_{27} + d_{20}$. Using K-Map and write logic diagram for reduced Boolean equation. **(10 Marks)**

2 a. Write truth table K-Map and logic diagram for half subtractor. **(04 Marks)**

b. Simplify $Q=f(v, w, x, y, z) = M_4 M_{12} M_{15} M_{17}$. Using Quine – Mc Clusky method. **(10 Marks)**

c. Two motor M_2 and M_1 are controlled by three sensors S_1, S_2 and S_3. M_2 is to run any time all three sensors are on (true). The other motor is to run whenever sensors S_2 or S_1 but not both are on and S_3 is off. For all sensor combinations where M_1 is on M_2 is to be off except when all three sensors are off and then both motors must be off. Write Boolean output equations. **(06 Marks)**

3 a. Define explain decoder. **(05 Marks)**

b. Implement full subtractor using 74138 and NAND gate only. **(08 Marks)**

c. Define and explain digital MUX. **(07 Marks)**

4 a. Realize Boolean equation $T= f(w, x, y, z) = \Sigma m(1, 2, 5, 7, 12, 14)$, Using 8 to 1 MUX. **(08 Marks)**

b. List the steps of general approach to combinational logic design. **(06 Marks)**

c. Write a note on cascading type 1 bit comparator with truth table and diagram. **(06 Marks)**

5 a. Write a note on SR latch using NAND gate. **(05 Marks)**

b. Write characteristics table, excitation table characteristics equation of JK flip-flop. **(07 Marks)**

c. Compare Moore model and Mealay model to representing sequential machines. **(08 Marks)**

6 a. Implement Divide by 8 Binary ripple counter using JK flip-flop 7476. Write timing diagram and logic diagram. **(07 Marks)**

b. Design synchronous self starting Mod-6 upcounter using T flip-flop. **(09 Marks)**

c. Explain shift right and shift left operations with figure for registers block. **(04 Marks)**

7 a. Write transition table for given state diagram (Ref. Fig Q7(a)).

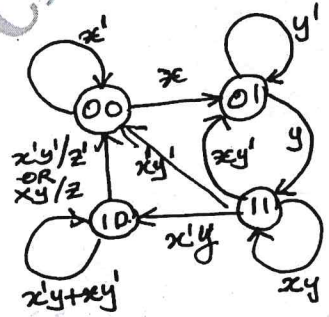

Fig Q7(a) **(08 Marks)**

b. List the steps of synchronous sequential circuit analysis. **(12 Marks)**

8 a. Write transition excitation table state table, state diagram and timing diagram for the sequential machine given in Fig Q8(a).

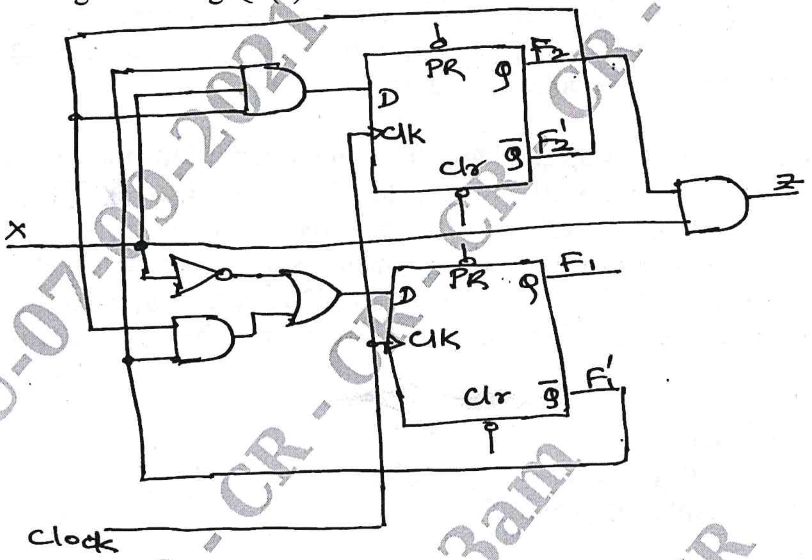

Fig Q8(a) **(12 Marks)**

b. Write a note one decade up counter. **(08 Marks)**

9 a. Write a note on Data types used in VHDL with examples and specifications. **(08 Marks)**
b. What are the fundamental sections that comprise a VHDL code? Explain with any example code. **(12 Marks)**

10 a. Explain how VHDL evolved in early stages of development. **(09 Marks)**
b. Write note on Major capabilities of verilog. **(11 Marks)**

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