CBCS Scheme

USN | | | | | | | | | | |

15EC33

Third Semester B.E. Degree Examination, June/July 2017
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Convert the given Boolean function into
i) $Y = f(a, b, c) = (a + b)(a + c)$ minterm canonical form **(04 Marks)**
ii) $P = f(a, b, c) = (a + b)(b + c)(\overline{c} + a)$ maxterm canonical form. **(04 Marks)**

b. Using K-map determine the minimal sum of product expression and realize the simplified expression using only NAND gates.
$M = f(W, X, Y, Z) = \sum (1, 4, 5, 6, 11, 12, 13, 14, 15)$. **(08 Marks)**

OR

2 a. Simplify the given Boolean function using Quine – McCluskey method :
$Y = f(a, b, c, d) = \sum (0, 2, 3, 5, 8, 10, 11)$. Verify the result using k-map. **(12 Marks)**

b. Distinguish between prime implicant and Essential prime implicant. **(04 Marks)**

Module-2

3 a. Define Decoder. Implement the following multiple output function using IC 74138 and external gates. Also write the truth table.
$P = f_1 (X, Y, Z) = \sum (1, 2, 5, 6)$
$Q = f_2 (X, Y, Z) = \pi (3, 5, 6, 7)$. **(06 Marks)**

b. Implement the following Boolean function using 8:1 multiplexer :
$Y = f(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$ **(10 Marks)**

OR

4 a. Design and implement 4-bit look ahead carry adder. **(08 Marks)**

b. Design and implement BCD to Excess-3 code converter. **(08 Marks)**

Module-3

5 a. Explain the working principle of gated SR latch. **(06 Marks)**

b. Explain the working of master slave JK flip-flop with the help of a logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

OR

6 a. With a neat logic diagram, explain the working of positive edge triggered D flip-flop. Also draw the timing diagram. **(08 Marks)**

b. Derive the characteristic equation for JK and T flip-flop. **(08 Marks)**

Module-4

7 a. Describe the working principle of universal shift register with the help of logic diagram and mode control table. **(08 Marks)**

b. Illustrate the operation of 4-bit binary ripple counter using logic diagram and timing diagram. **(08 Marks)**

OR

8 a. Design a synchronous Mod-6 counter using clocked T flip-flop. **(10 Marks)**

b. Explain Mod-4 ring counter using D flip-flop. **(06 Marks)**

Module-5

9 a. Explain Mealy and Moore sequential circuit models. **(04 Marks)**

b. For the logic diagram shown in Fig Q 9(b).

i) Write input and output equations

ii) Construct transition table

iii) Draw state diagram. **(12 Marks)**

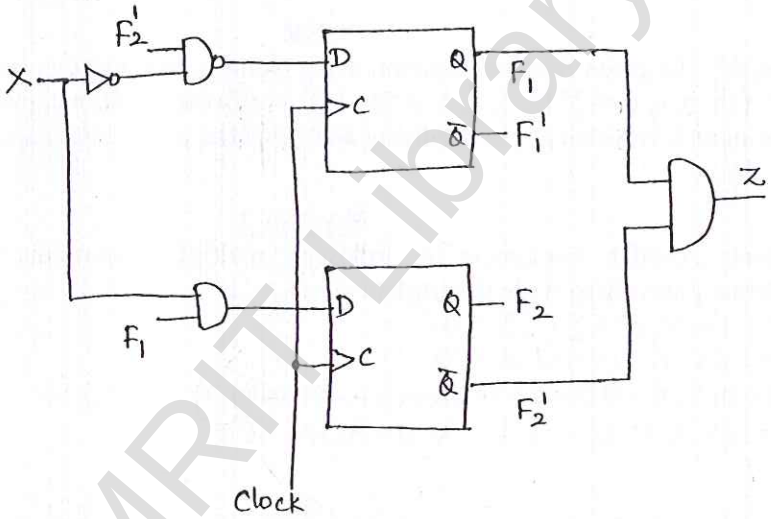

Fig Q9(b)

OR

10 a. Define the terms as applied to sequential circuit :
Input variable, output variable, Excitation variable and state variable. **(04 Marks)**

b. Design a sequential circuit for a state diagram shown in Fig Q 10(b). **(12 Marks)**

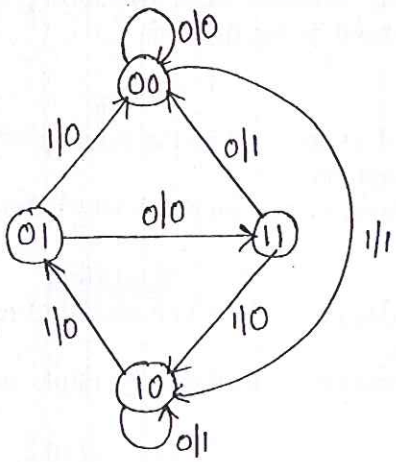

Fig Q10(b)

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