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10EC56

Fifth Semester B.E. Degree Examination, June/July 2017
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Describe in detail the step-by-step procedure involved in the fabrication of nMOS. **(08 Marks)**

b. Calculate the threshold voltage with $\epsilon_{si} = 11.7\,\epsilon_0$, $\epsilon_{ox} = 3.9\,\epsilon_0$ for an nMOS transistor with $Q_{fc} = 0$, $N_i = 1.45 \times 10^{10}/cm^3$, $N_A = 5\times10^{17}/cm^3$, $t_{ox} = 150\,Å$ and $\phi_{ms} = -0.9V$ using the equation $V_t = V_{tmos} + V_{fb}$. Plot the graph of 'V_t' versus 't_{ox}' for t_{ox} ranging from 50 Å to 300 Å and interpret the graph. **(06 Marks)**

c. With the truth table, draw the schematic for 2:1 MUX and 2-input XOR gate using transmission gate. **(06 Marks)**

2 a. List the colour, stick encoding, mask layout encoding for n-diffusion, p-diffusion, polysilicon metal 1 and metal 2. **(07 Marks)**

b. Draw the circuit and stick diagram for one-bit CMOS shift register. **(06 Marks)**

c. Draw the optimum layout of CMOS inverter whose $\left(\frac{W_p}{W_n}\right) = \frac{4}{2}$ by stitching the source and drain regions of 2:1 inverter with the contacts and metal. Discuss the merits of such design. Given $L_p = L_n = 1$. [Hint : Placing the transistor back to back]. **(07 Marks)**

3 a. Write the voltage-current equations for nMOS and pMOS transistor, with V-I characteristics discuss channel length modulation. **(08 Marks)**

b. Realize the boolean equation using CMOS and C^2MOS logic $Z = \overline{A(B+C)+DE}$ **(06 Marks)**

c. Discuss BiCOMS logic and CMOS domino logic with relevant schematic. **(06 Marks)**

4 a. Discuss the limits of scaling
   i) Substrate doping
   ii) Limits on miniaturization
   iii) Limits on interconnect and contact resistance. **(06 Marks)**

b. Describe the possible effect of propogation delay in cascaded pass transistors and long polysilicon wires. **(06 Marks)**

c. Calculate the area capacitance of a multilayer structure shown in Fig Q4(a), if feature size = 5 μm and relative value of metal to substrate = 0.075, polysilicon = 0.1, diffusion = 0.25. **(08 Marks)**

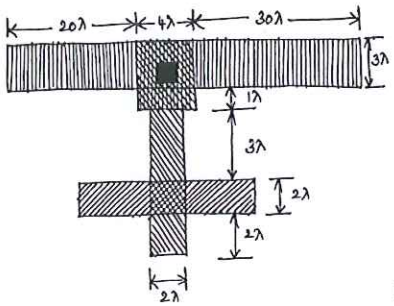

Fig 4(c)

PART – B

5 a. Discuss the architectural issues to be followed in the design of a VLSI subsystem. **(08 Marks)**

b. Show an arrangement to generate any logic function of two variable (A, B) by programming the inputs $I_0 - I_3$ appropriately with 0's and 1's using 4-way multiplexer. **(08 Marks)**

c. Define Metastability. Find the MTBU (t_f) of a system given f_c = 50MHz, f_d = 100KHz, t_f = 10ns, T_0 = 0.1s, τ_r = 0.2ns using the equation MTBU (t_f) = $\frac{1}{f_c f_d T_o e^{\frac{-t_f}{\tau_r}}}$. **(04 Marks)**

6 a. Design a 4-bit serial-parallel multiplier. **(10 Marks)**

b. Derive carry look – ahead adder equations and design a 4-bit CLA adder with a combination of ripple-through, given the following equation for carry and sum is

$C_k = A_k \cdot B_k + (A_k + B_K) C_{k-1}$

$S_k = A_k \cdot B_k + B_k \cdot C_k + C_k \cdot A_k$

Where A, B, C are input variables and K = {0, 1, 2, . . . n-1}. **(10 Marks)**

7 a. Discuss the various system timing considerations. **(06 Marks)**

b. Describe the working of CMOS pseudo static RAM cell. Determine the area requirement, estimated dissipation per bit stored and volatility of the same. **(08 Marks)**

c. Draw the schematic of 6-transistor SRAM cell. Discuss read 'O' and write 'O' operations with appropriate schematic diagrams. **(06 Marks)**

8 a. Mention the types of I/O pads and discuss their functionalities. **(08 Marks)**

b. Discuss noise margin in CMOs technology for a cascaded inverters (set of 2). Draw the noise margin graphs indicating NM_H, NM_L, V_{OH}, V_{IL}, V_{OL} and V_{IH} **(08 Marks)**

c. From the Figure Q 8(c) shown below, identify appropriate widths for nMOS and pMOS transistors to obtain optimum delay and area. **(04 Marks)**

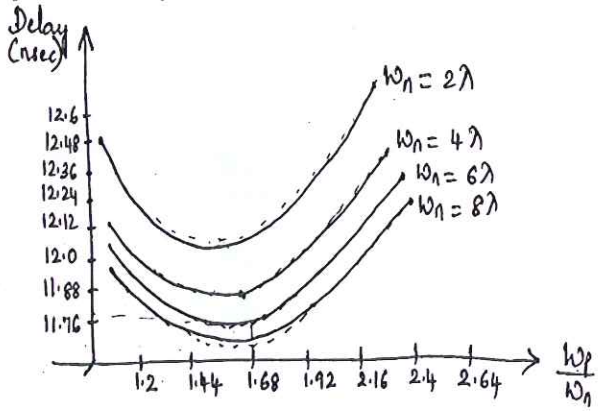

Fig Q8(c)

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