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10EC666

Sixth Semester B.E. Degree Examination, June/July 2017
Digital System Design using Verilog

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Define digital system and briefly explain the needs for digital systems. **(05 Marks)**

b. What do you mean by logic levels in digital systems? Explain the TTL logic levels with noise margins. **(08 Marks)**

c. Explain the embedded system design with the help of flowchart. **(07 Marks)**

2 a. Define bit error and explain the generation and checking of parity bit for 8 bit code with circuits. **(10 Marks)**

b. Develop a verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit. **(10 Marks)**

3 a. Develop a verilog behavioral model of an adder/subtractor for 12 bit unsigned binary numbers. The circuit has data inputs x and y, a data output s, a control input mode that is 0 for addition and 1 for subtraction, and an output ovf_unf that is 1 when an addition overflow or a subtraction under flow occurs. **(05 Marks)**

b. Explain the floating point numbers with an example. **(05 Marks)**

c. Develop an verilog code to convert from binary code to gray code. **(10 Marks)**

4 a. Develop a verilog model for an interval timer that has clock, load and data input ports and a terminal-count output port. The timer must be able to count intervals of upto 1000 clock cycles, when it reaches zero, it reloads the previously loaded value rather than wrapping around to the largest count value. **(07 Marks)**

b. Explain the FSM circuit structure. **(05 Marks)**

c. What are asynchronous inputs? Briefly explain the effect of those inputs on digital design and also mention the possible solution. **(08 Marks)**

PART – B

5 a. Explain asynchronous and synchronous static RAM with timing waveforms. **(10 Marks)**

b. Compute the 12 bit ECC word corresponding to the 8 bit data word 01100001. **(05 Marks)**

c. Write a note on ASIC concept. **(05 Marks)**

6 a. Briefly explain the different arithmetic, logical and shift instructions from Gumnut instruction set. **(12 Marks)**

b. Briefly explain the different techniques, which enable a higher rate of data transfer or memory bandwidth. **(08 Marks)**

7 a. What are the serial interface standards? Explain any four, **(10 Marks)**

b. Mention the needs for ADC and DAC in I/O interfacing. **(04 Marks)**

c. Write a note on polling and timers. **(06 Marks)**

8 a. Define DFT and BIST, design a 4 bit LFSR for generating pseudo-random test vectors. **(10 Marks)**

b. Explain area and timing optimization. **(10 Marks)**

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