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10TE74

Seventh Semester B.E. Degree Examination, June/July 2017

DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain a digital signal processing system with the help of a block diagram. **(06 Marks)**

b. Explain the decimation and interpolation process with an example. **(08 Marks)**

c. An analog signal is sampled at the rate of 8 kHz. If 512 samples of this signal are used to compute the Fourier transform X(K), determine the frequency spacing between adjacent X(K) elements. Also, determine the analog frequency corresponding to K = 64, 128 and 200. **(06 Marks)**

2 a. Bring out the basic features that should be provided in a DSP architecture to carry out N^{th} order FIR filter operation. **(08 Marks)**

b. Explain how the circular addressing mode and bit reversal addressing mode are implemented in a digital signal processor. **(08 Marks)**

c. How many bits should the accumulator be, so that the sum of 100 unsigned numbers represented by a 16 bits each can be computed without the occurance of overflow error or loss of accuracy? **(04 Marks)**

3 a. Explain with block diagram, the direct addressing mode of TMS320C54XX processor. **(08 Marks)**

b. Explain the program control unit of TMS320C54XX processor. **(06 Marks)**

c. With a neat functional diagram, explain the band shifter of the TMS320C54XX processor. **(06 Marks)**

4 a. Explain the six-stage pipeline structure of TMS320C54XX execution. **(08 Marks)**

b. Write about the different types of serial ports available on C54XX devices. **(06 Marks)**

c. What will be the contents of the following, after the execution of the instruction:

MACD *AR3_, COEFFS, A.

All the values are in hexadecimal.

A : 00	0077	0000
T :		0008
FRCT :		0
AR3 :		0100
Program memory		
Coeffs :		1234
DATA memory		
0100h :		0055
0101h :		0060

(06 Marks)

PART – B

5 a. Represent each of the following as 16 bit number in the desired Q-notation:
   i) 0.3125 as Q_{15} number
   ii) -0.3125 as Q_{15} number
   iii) 3.125 as Q_7 number
   iv) -352 as Q_0 number **(06 Marks)**

   b. What is an interpolating filter? Write a TMS320C54XX program to implement an interpolating filter using a 15 tap FIR filter and an interpolating factor of 5. **(14 Marks)**

6 a. Determine the following for a 128-point FFT computation:
   i) Number of stages
   ii) Number of butterflies in each stage
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that need no twiddle factors
   v) Number of butterflies that require real twiddle factors
   vi) Number of butterflies that require complex twiddle factors. **(06 Marks)**

   b. Explain how scaling prevents overflow condition in butterfly computation. **(06 Marks)**

   c. Write the subroutine for bit reverse address generation and explain. **(08 Marks)**

7 a. Explain DMA with respect to TMS320C54XX processor. **(08 Marks)**

   b. With neat sketches, explain the memory space organization of TMS320C5416 processor. **(08 Marks)**

   c. For a C5416 processor with 23 bit address lines, the least 13 bits are used to interface an external program memory. How many address ranges exist for each location to access this external program memory? **(04 Marks)**

8 a. Explain JPEG encoding and decoding with the help of a block diagram. **(10 Marks)**

   b. With a neat block diagram and timing diagram, for both transmit and receive, explain the signals involved in synchronous serial interface. **(10 Marks)**

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