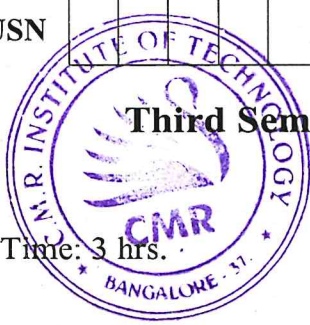


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Third Semester B.E. Degree Examination, July/August 2021

Digital System Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- 1
 - a. Define combinational logic circuit and place the following equation into the proper canonical form:
 $P = f(a, b, c) = ab' + ac' + bc$ (04 Marks)
 - b. Obtain minimal expression using k-map for the following incompletely specified function:
 $F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw the circuit diagram using basic gates. (06 Marks)
 - c. Minimize the expression using Quine Mecluskey method.
 $Y = \overline{A}BCD + \overline{A}BC\overline{D} + A\overline{B}CD + A\overline{B}C\overline{D} + \overline{A}BCD + \overline{A}B\overline{C}D$ (10 Marks)

- 2
 - a. Place the following equations into the proper canonical form:
 - i) $G = f(w, x, y, z) = \overline{w}x + y\overline{z}$
 - ii) $T = f(a, b, c) = (a + \overline{b})(\overline{b} + c)$ (04 Marks)
 - b. Obtain minimal logical expression for the given maxterm expression using K-map
 $f(a, b, c, d) = \pi M(0, 1, 4, 5, 6, 7, 9, 14) \cdot \pi d(13, 15)$. (06 Marks)
 - c. Obtain all the prime implicants of the following Boolean function using Quine-Meckluskey method
 $f(a, b, c, d) = \sum(0, 2, 3, 5, 8, 10, 11)$. Verify the result using K map technique. (10 Marks)

- 3
 - a. Draw the circuit for 3 to 8 decoder and explain. (08 Marks)
 - b. Implement the following Boolean function using 4:1 multiplexer.
 $F[A, B, C, D] = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. (06 Marks)
 - c. A combinational circuit is defined by the functions $F_1 = \sum m(3, 5, 7)$, $F_2 = \sum m(4, 5, 7)$. Implement the circuit with a programmable logic array having 3 inputs, 3 product terms and two outputs. (06 Marks)

- 4
 - a. Draw the key pad interfacing diagram to a digital system using 10-line decimal to BCD encoder and explain. (06 Marks)
 - b. Explain Look-Ahead carry adder with neat diagram and relevant expression. (06 Marks)
 - c. Design 2-bit comparator using gates. (08 Marks)

- 5
 - a. Explain the operation of a switch debouncer using S-R. Latch with the help of circuit and waveforms. (06 Marks)
 - b. Find characteristic equations for S-R and T. Flip flops with the help of function tables and explain. (06 Marks)
 - c. Explain the working principle of 4-bit synchronous binary counts. (08 Marks)

- 6 a. Draw the logic diagram, functional table and timing diagram of master-slave JK flip flop and explain briefly. (10 Marks)
 b. Explain four bit binary ripple counter with logic and timing diagram. (10 Marks)
- 7 a. Design mod-6 synchronous counter by using JK flip-flop, with excitation table. (10 Marks)
 b. Draw and explain Mealy and Moore sequential circuit model and compare mealy and Moore circuit models. (10 Marks)
- 8 a. Design a Mod-6 synchronous counter using clocked T Flip-Flop. (10 Marks)
 b. Construct the transition table, state table and state diagram for the sequential circuit shown in Fig.Q.8(b). (10 Marks)

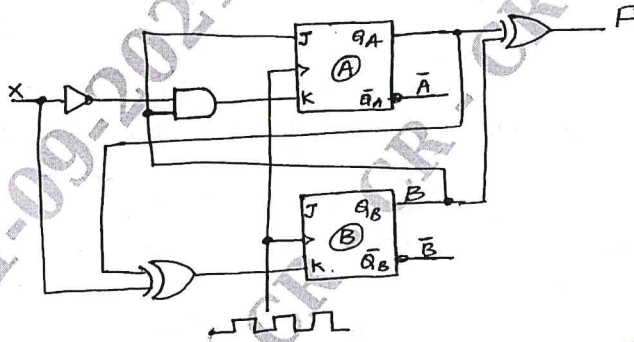


Fig.Q.8(b)

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- 9 a. Design and draw Mealy model of sequential detector circuit to detect the pattern 101. (10 Marks)
 b. Draw the block diagram of serial adder with accumulator and explain its working operation. (10 Marks)
- 10 a. State the guidelines for construction of state graph. (06 Marks)
 b. Draw the block diagram of binary multiplier and explain its working principle. (08 Marks)
 c. Draw and explain the operation of FPGA implementation of a parallel adder with accumulator. (06 Marks)
