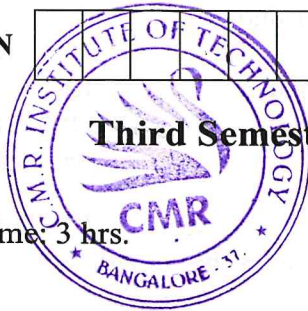


CBCS SCHEME

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17EC33



Third Semester B.E. Degree Examination, July/August 2021 Analog Electronics

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions.

1.
 - a. Mention the steps involved for obtaining the AC equivalent of a transistor network. (04 Marks)
 - b. Derive an expressions for input impedance, output impedance and voltage gain for CE fixed bias configuration using r_e equivalent model. (08 Marks)
 - c. Define hybrid parameters and explain hybrid π model with neat sketch. (08 Marks)
2.
 - a. Draw the circuit diagrams, for transistor r_e model in common Emitter and common base configuration. (04 Marks)
 - b. Derive expressions for Z_i , Z_o , A_v and A_i for emitter follower configuration using approximate hybrid equivalent model. (08 Marks)
 - c. For the network shown in Fig.Q2(c), without C_E (unbypassed), determine r_e , Z_i , Z_o and A_v .

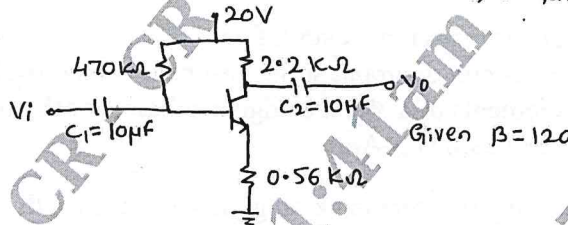


Fig.Q2(c)

(08 Marks)

3.
 - a. Mention the differences between JFET and MOSFET. (04 Marks)
 - b. Explain with neat sketches operation and characteristics of n-channel enhancement MOSFET. (08 Marks)
 - c. Find r_d , Z_i , Z_o , and A_v for the circuit shown in Fig.Q3(c).

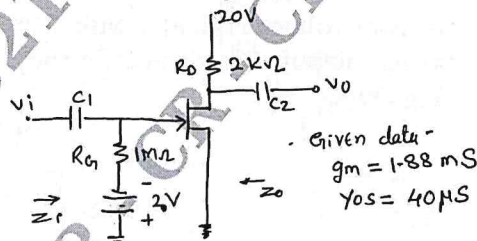


Fig.Q3(c)

(08 Marks)

4.
 - a. Sketch the following circuit diagrams :
 - i) JFET AC equivalent model of source follower
 - ii) Cascaded FET amplifier. (04 Marks)
 - b. Derive an expressions for Z_i , Z_o , and A_v using small signal JFET amplifier for self bias configuration (Bypassed R_s). (08 Marks)
 - c. For the source follower network shown in Fig.Q4(c), determine : i) r_d ii) Z_i iii) Z_o iv) A_v .

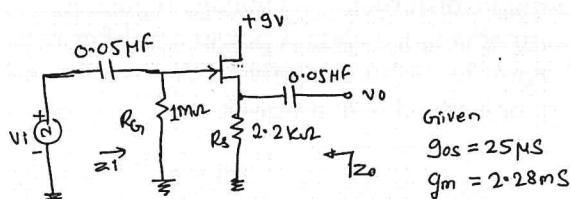


Fig.Q4(c)

(08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

- 5 a. An amplifier rated at a 40W output is connected to a $10\ \Omega$ speaker find :
 i) Input power required for full output if power gain is 25dB
 ii) Input voltage for rated output if the amplifier voltage gain is 40dB. (06 Marks)
- b. Explain high frequency response of JEFT amplifiers. (08 Marks)
- c. Explain multistage frequency effects. (06 Marks)
- 6 a. Derive an expressions for Miller input and output capacitors. (06 Marks)
- b. Determine r_e , A_V and R_i for the low frequency response of BJT amplifier circuit shown in Fig.Q6(b). Assume $r_0 = \infty$.

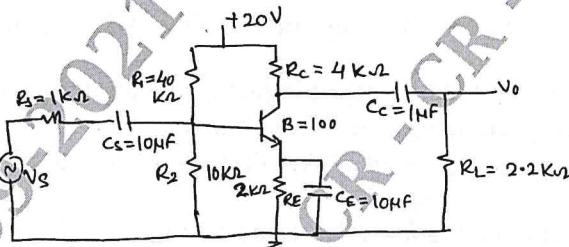


Fig.Q6(b)

(08 Marks)

- c. Draw the circuit diagram of :
 i) High frequency response of BJT amplifier in CE mode with capacitances effects
 ii) Low frequency response of FET amplifier in common source mode with capacitive elements effects. (06 Marks)
- 7 a. List the conditions for sustained oscillations. (04 Marks)
- b. Explain with neat circuit diagram, series resonant crystal oscillator using BJT. (08 Marks)
- c. Design the RC elements of a Wein bridge oscillator for the operation at $f = 10\text{KHz}$ and draw the oscillator circuit using op-Amp. (08 Marks)
- 8 a. Explain effect of negative feedback on gain and Bandwidth. (05 Marks)
- b. Explain with neat circuit diagram, the operation of BJT Colpitt oscillator and mention its advantages over Hartely oscillator. (08 Marks)
- c. Explain UJT relaxation oscillator with necessary equations and waveforms. (07 Marks)
- 9 a. Classify the power amplifiers and define them with necessary waveforms and 'Q' point. (06 Marks)
- b. Explain series transistor voltage regulator with neat diagram. (06 Marks)
- c. Calculate input power, output power and efficiency of the series fed class A power amplifier circuit shown in Fig.Q9(c).

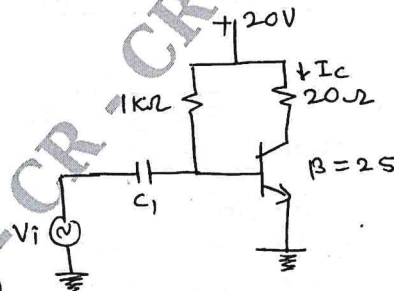


Fig.Q9(c)

(08 Marks)

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- 10 a. Define : i) Cross over distortion ii) percentage voltage regulation iii) amplifier efficiency
 iv) harmonic distortion v) voltage regulator. (10 Marks)
- b. Explain transformer coupled class A power amplifier with necessary equations. (06 Marks)
- c. For class 'B' amplifier using a supply of $V_{CC} = 30\text{V}$ and driving a load of $16\ \Omega$, determine maximum input power and output power. (04 Marks)