17EC53 Semester B.E. Degree Examination, July/August 2021
Verilog HDL Max. Marks: 100

1	BANC	Note: Answer any FIVE full questions.		
1	a.	Explain the typical design flow for designing VLSI IC circuits.	(10 Marks)	
	b.	Discuss the evaluation of computer aided design.	(05 Marks)	
	c.	Explain top-down design methodology.	(05 Marks)	
_		P: 11 :	(40 % / 1-)	
2	a.	Discuss modules, instances with the help of 4-bit ripple carry counter example.	(10 Marks)	
	b.	Describe instance and instantiation with example.	(05 Marks)	
	c.	Explain stimulus and design block with an example.	(05 Marks)	
•		Discount of the data to a solid a solid an extended	(10 Mayles)	
3	a.	Discuss the data types used in verilog with an example.	(10 Marks)	
	b.	Explain system task and compiler directives in verilog.	(10 Marks)	
4	2	Explain components of verilog module with an example.	(10 Marks)	
4	a. b.	Explain port declaration, port connection rules and connecting ports to external si		
	υ.	Explain port declaration, port connection rules and connecting ports to external si	(10 Marks)	
5		Write a verilog gate level description for 4:1 multiplexes also write stimulus bloc		
3	a.	Write a verified gate level description for 4.1 multiplexes also write stimulus offer	(10 Marks)	
	b.	Explain rise delay, fall delay, turn off delay, min value, typical value and max val		
	υ.	Emplain his actuy, tan actuy, tan	(10 Marks)	
6	a.	Describe continuous assignment statement and implicit continuous assignment statement.		
	.2		(10 Marks)	
	b.	Explain arithmetic and logical operators with example.	(10 Marks)	
			(1035 1)	
7	a.	Explain blocking and non blocking procedural assignment in behavioral modeling	- 1001 O	
	b.	Describe event-based-timing control mechanism in behavioral modeling.	(10 Marks)	
		The state of the s		
8	a.	Explain conditional statements. Using if and else write a verilog HDL program for	(10 Marks)	
	16	Describe multiway branching. Use case statement and write verilog program for		
	b.	counter.	(10 Marks)	
		counter.	(201.201.0)	
9	a.	Why we use VHDL? What are the short comings of VHDL?	(10 Marks)	
	b.	Describe the design in VHDL.	(10 Marks)	
	~ .		,	
10	a.	Discuss the basic building block of VHDL design with an example of dataflow/behavioral		
		description. (10 Marks)		
	h	Write a VHDI description for 4 hit ripple carry adder also write the circuit	diagram for	

b. Write a VHDL description for 4 bit ripple carry adder, also write the circuit diagram for (10 Marks) same.

CMRIT LIBRARY BANGALORE - 560 03?