

CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

15EC53

Fifth Semester B.E. Degree Examination, July/August 2021

Verilog HDL

Time: 3 hrs.

Max. Marks:80

Note: Answer any FIVE full questions.

- Explain a typical design flow for designing VLSI IC circuit using block diagram. (06 Marks)
 - Develop verilog code for 4-bit ripple carry counter and with neat block diagram explain design hierarchy for the same. (10 Marks)
- Explain top-down design methodology and bottom up design methodology. (10 Marks)
 - Explain the importance of HDL and also mention useful features of verilog HDL. (06 Marks)
- Explain the following data-types with an example in verilog :
i) Nets ii) Registers iii) Vectors iv) Arrays. (08 Marks)
 - Explain the below mentioned system tasks NAND compiler directives with examples :
i) \$display ii) \$monitor iii) 'Define iv) 'Include. (08 Marks)
- With a neat block diagram explain components of verilog module. (06 Marks)
 - Explain port connection rules. (06 Marks)
 - Write a verilog code for SR latch using and gates as elements. (04 Marks)
- What are rise, fall and turnoff delays? How they are specified in verilog. (06 Marks)
 - Design and develop verilog code for an 4-bit ripple carry adder using 1-bit fulladder as a component. Also write stimulus for 4-bit ripple carry fulladder. (10 Marks)
- For the schematic network shown below. Write a verilog code for gate level implementation with delay s mentioned :

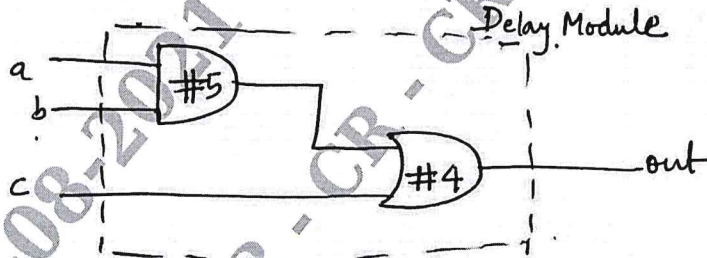


Fig.Q6(a)

- Also write stimulus for the above example. (06 Marks)
 - Write a verilog code for :
 - 2 : 1 mux with conditional operator
 - 4 : 1 mux with conditional operators
 - 4 : 1 mux using logic equation
 - 2 : 1 mux using logic equation. (10 Marks)
- Explain with examples always and initial statements. (08 Marks)
 - Explain blocking assignment statements and non-blocking assignment statements with relevant examples. (08 Marks)

15EC53

- 8 a. Explain sequential and parallel blocks with examples. (08 Marks)
b. Write a verilog code for :
i) 4 : 1 multiplexer using case statement
ii) 4 – bit counter with behavioral description. (08 Marks)
- 9 a. Explain design tool flow diagram with block diagram. (08 Marks)
b. i) Write VHDL dataflow description for – 4 – bit equality comparator using logic equations and block diagrams. (04 Marks)
ii) Write VHDL structural description for 4-bit comparator with necessary block diagrams. (04 Marks)
- 10 a. Explain the declaration of constant, variable and signal in VHDL, with example. (08 Marks)
b. Explain attributes in VHDL. (04 Marks)
c. Write a VHDL code for half adder using behavioral description. (04 Marks)

* * * * *

CMRIT LIBRARY
BANGALORE - 560 037