

Time: 3 hrs.

Sixth Semester B.E. Degree Examination, July/August 2021

Microelectronic Circuits

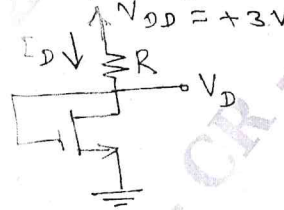
Max. Marks:100

Note: Answer any FIVE full questions.

- 1 a. Draw drain current versus drain-to source voltage characteristic for an enhancement-type NMOS, Mark all regions and explain it. (06 Marks)

- b. Design a MOSFET circuit show in Fig.Q.1(b) to obtain a current I_D of $80\mu\text{A}$. Find the value required for R and find the dc voltage V_D . Let the NMOS transistor have $V_t = 0.6\text{V}$, $\mu_n C_{ox} = 200\mu\text{A}/\text{V}^2$, $L = 0.8\mu\text{m}$ and $W = 4\mu\text{m}$. Neglect the channel length modulation effect.

Fig.Q.1(b)



- c. Explain the development the T-equivalent circuit model for the MOSFET and also body effect. (08 Marks)
- 2 a. For the NMOS transistor with $W/L = 10$ fabricated in the $0.18\mu\text{m}$ process. Find: i) The values of V_{OV} and V_{GS} required to operate the device at $I_D = 100\mu\text{A}$; ii) V_{BE} for an npn transistor fabricated in the low-voltage process and operated at $I_C = 100\mu\text{A}$. Assume $\mu_n C_{ox} = 387\mu\text{A}/\text{V}^2$, $V_{tn} = 0.48\text{V}$, $I_S = 6 \times 10^{-18}\text{A}$ and $V_T = 0.02\text{sv}$. (06 Marks)
- b. Explain the process of generating bias current for different amplifier stages of various amplitudes. (06 Marks)
- c. Derive the expression of upper 3-dB frequency of an amplifier and also find the 3-dB frequency of a

$$F_H(s) = \frac{1 - \frac{s}{10^3}}{\left(1 + \frac{s}{10^4}\right) \left(1 + \frac{s}{4 \times 10^4}\right)} \quad (08 \text{ Marks})$$

- 3 a. For the common gate amplifier $W/L = 7.2\mu\text{m}/0.36\mu\text{m}$, $\mu_n C_{ox} = 387\mu\text{A}/\text{V}^2$, $r_o = 18\text{K}\Omega$, $I_D = 100\mu\text{A}$, $g_m = 1.25\text{mA}/\text{V}$, $\chi = 0.2$, $R_S = 10\text{K}\Omega$, $R_L = 100\text{K}\Omega$, $C_{gs} = 20\text{fF}$, $C_{gd} = 5\text{fF}$, $C_L = 0$, find A_{v_o} , R_{in} , R_{out} , G_v , G_{is} , G_i and f_H . (08 Marks)
- b. Explain the high frequency response of the CS-amplifier using open circuit time constants and also obtain 3-dB frequency. (08 Marks)
- c. What is cascade amplifier? Explain the basic idea behind the cascade amplifier. (04 Marks)
- 4 a. Explain the working of a Wilson current mirror and derive the expression of current transfer ratio. (08 Marks)
- b. The differential amplifier shown in Fig.Q.4(b) uses transistors with $B = 100$, determine:
- Input differential resistance R_{id}
 - Over all differential voltage gain
 - Worst-case common-mode gain if the two collector resistances are accurate to within $\pm 1\%$
 - CMRR. (08 Marks)

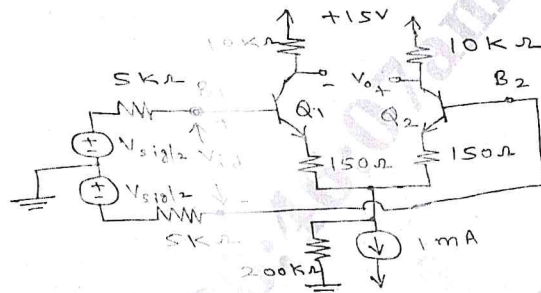


Fig.Q.4(b)

- c. Mention the reasons why differential amplifiers are well suited for IC fabrications. (04 Marks)
- 5 a. Derive the expression of a CMRR of a active loaded MOS differential amplifier. (08 Marks)
- b. Explain the main functions of multistage amplifier. (06 Marks)
- c. Draw the circuit of a differential to single ended conversion and explain it. (06 Marks)
- 6 a. Draw the block diagram of a shunt-shunt feedback and derive the expression of input resistance and output resistance with feedback. (08 Marks)
- b. Discuss the effect of feedback on the amplifier poles. (06 Marks)
- c. Discuss the properties of negative feedback with mathematical analysis. (06 Marks)
- 7 a. Using the superposition principle to find the output voltage of the circuit shown in Fig.Q.7(a). (04 Marks)

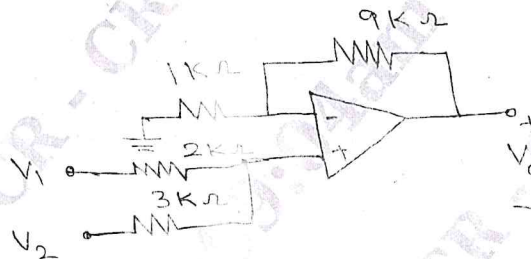


Fig.Q.7(a)

- b. What are the major disadvantages of instrumentation amplifier using op-amp? (04 Marks)
- c. For the circuit shown in Fig.Q.7(c) derive an expressions for the transfer function $V_0(s)/V_1(s)$, dc gain and the 3-dB frequency. (06 Marks)

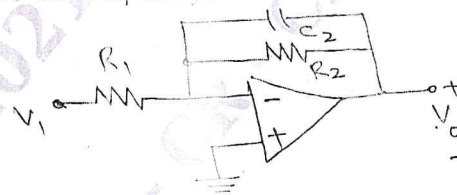


Fig.Q.7(c)

- d. Draw the circuit diagram of sample and hold circuit using op-amp and explain it. (06 Marks)
- 8 a. Discuss the reasons for CMOS displacing bipolar technology in digital applications. (04 Marks)
- b. Implement the following Boolean expression:
 - i) $F = (\overline{A+B})(C+\overline{D})$ using OAI gate logic. (08 Marks)
 - ii) $F = \overline{AB+CD}$ using AOI gate logic. (08 Marks)
- c. Explain the transistor sizing in CMOS gate circuits. (08 Marks)
