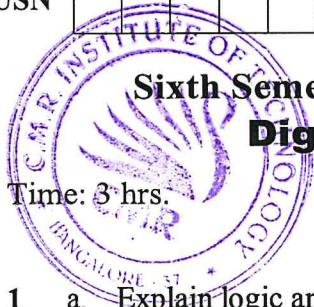


CBCS SCHEME

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15EC663



Sixth Semester B.E. Degree Examination, July/August 2021 Digital System Design Using Verilog

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions.

- 1 a. Explain logic and static load levels constraints imposed in Real World circuits. (08 Marks)
b. Develop a verilog model for a 7-segment decoder, that includes an additional input "BLANK" that overrides the BCD input and causes all segments not to be lit. (08 Marks)
- 2 a. What is state transition diagram? Explain with Moore and Mealy style output values. (08 Marks)
b. Develop a verilog model of a debouncer for a push button switch that uses a debounce interval of 10ms. Assume the system clock frequency is 50MHz. (08 Marks)
- 3 a. Explain Asynchronous static RAM timing methodology. (08 Marks)
b. Develop a verilog model of a dual port, $4K \times 16$ bit flow – through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. (08 Marks)
- 4 a. Explain different types of ROMS. (08 Marks)
b. Design a $64K \times 8$ bit composite memory using $4-16K \times 8$ bit components. (08 Marks)
- 5 a. Explain internal circuit of a PAL16L8 component. (08 Marks)
b. Design and explain the circuit for a slice within a logic block of Xilinx Spartan – II FPGA. (08 Marks)
- 6 a. What design techniques can be used to Mitigate Transmission – line effects, such as over shoot, undershoot and ringing? (04 Marks)
b. Briefly explain internal organization of CPLD. (04 Marks)
c. Design a priority encoder that has 16 inputs, $I[0:15]$; a 4-bit encoded output, $Z[3:0]$; and a valid output that is '1' when any input is '1'. Input $I[0]$ has the highest priority and $I[15]$ the lowest priority. The design is to be implemented in a GAL22V10 component. (08 Marks)
- 7 a. Explain four different serial interface standards. (08 Marks)
b. Explain how we could decode a BCD value to drive the seven segments of a digit. (08 Marks)
- 8 a. Explain the following I/O synchronization techniques i) Polling ii) Timers. (06 Marks)
b. With a neat sketch describe R-string DAC. (06 Marks)
c. Explain distributed Multiplexer bus standard. (04 Marks)
- 9 a. Explain the purpose of floor planning, placement and routing of physical Design. (06 Marks)
b. Explain JTAG boundary scan cell for an input or output pin. (06 Marks)
c. Explain Hardware Abstraction Layer (HAL) Instruction Set Simulator (ISS) for Embedded System Software in brief. (04 Marks)
- 10 a. Explain 4-bit CFSR for generating Pseudo – random test vectors of BIST concept. (08 Marks)
b. What changes must be made to a circuit to create a scan chain? Explain in detail. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. $42+8=50$, will be treated as malpractice.