

CBCS SCHEME

USN

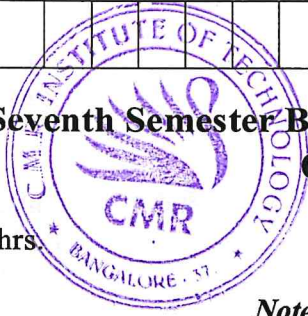
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15TE73

Seventh Semester B.E. Degree Examination, July/August 2021 CMOS VLSI Design

Time: 3 hrs

Max. Marks: 80



Note: Answer any FIVE full questions.

- 1 a. Derive the CMOS inverter DC characteristics highlighting the regions of operations. (10 Marks)
b. Write a note on evolution of IC era. (06 Marks)
- 2 a. Explain the steps involved in fabrication of nMOS, with neat diagrams. (10 Marks)
b. Explain the action of enhancement mode transistor for different values of V_{gs} and V_{ds} . (06 Marks)
- 3 a. Give the λ -based design rules for different layers, p and n MOSFETS and contact cuts. (08 Marks)
b. Draw the schematic and stick diagram of CMOS 2-input Nand gate, CMOS 2-input Nor gate. (08 Marks)
- 4 a. Define sheet resistance, sheet capacitance. (06 Marks)
b. Obtain the expression for total delay for N stages of nMOS and CMOS inverters in terms of width factor f and delay τ . (08 Marks)
c. Draw the schematic of $\overline{A+B+C}$ using NMOS technology. (02 Marks)
- 5 a. Write the scale factors for the following parameters:
 - i) Gate capacitance
 - ii) Maximum operating frequency
 - iii) Current density (J)
 - iv) Power speed product (P_T). (08 Marks)
b. What are the general considerations to be followed in designing a subsystem? (08 Marks)
- 6 a. Explain the various steps involved in designing a 4-bit adder. (08 Marks)
b. Explain Manchester carry-chain element with expressions for inputs and outputs. (08 Marks)
- 7 a. Explain structured design approach for a parity generator. (08 Marks)
b. Design a 4:1 multiplexer using nMOS logic and CMOS logic. (08 Marks)

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- 8 a. Explain the architecture of field programmable gate array. (08 Marks)
b. Discuss the FPGA abstractions with a diagram. (08 Marks)
- 9 a. Write and explain 4 transistor dynamic and 6 transistor static CMOS memory cell with sense amplifier. (10 Marks)
b. What are the timing considerations in system design? (06 Marks)
- 10 a. Write a note on test and testability. (08 Marks)
b. Discuss the requirements of I/O pads in a chip. (05 Marks)
c. Discuss observability and controllability. (03 Marks)

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