CBCS SCHEME

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17TE73

Seventh Semester B.E. Degree Examination, July/August 2021
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Explain the DC transfer characteristics of complementary CMOS inverter and highlight the regions of operations of MOS transistors. **(10 Marks)**

b. Explain nMOS fabrication process with neat diagram. **(10 Marks)**

2 a. Explain the following:
i) Channel length modulation
ii) Subthreshold conduction. **(10 Marks)**

b. Compare CMOS and Bipolar technologies. **(05 Marks)**

c. Explain the operation of CMOS tristate inverter with neat diagram. **(05 Marks)**

3 a. Draw circuit, stick and layout diagram for nMOS shift register cell. **(08 Marks)**

b. Explain 'λ' based design rules for contact cuts and vias with neat diagram. **(08 Marks)**

c. Define sheet resistance 'R_s' and standard unit of capacitance □Cg. Estimate the value of capacitance in □Cg for the given metal layer shown in Fig.Q.3(c), if features size is 2λ × 2λ and relative value of metal to substrate = 0.075. **(04 Marks)**

Fig.Q.3(c)

4 a. Draw the stick diagram for 4:1 nMOS inverter. **(06 Marks)**

b. Interpret Rise time and Fall time for CMOS Inverter. **(06 Marks)**

c. Explain Inverting and Non-Inverting super buffer. **(08 Marks)**

5 a. Determine the scaling factors the following:
i) Gate are 'Ag' and Gate capacitance 'Cg'
ii) Carrier density in channel 'Q_{on}'
iii) Saturation current 'Id_{ss}'
iv) Maximum operating frequency 'fo'
v) Power dissipation per gate 'Pg'. **(10 Marks)**

b. Explain 4 × 4 barrel shifter with neat diagram. **(10 Marks)**

6 a. Explain 4 bit data path for the processor with neat diagram. **(06 Marks)**

b. Develop 4 bit ALU to implement addition, subtraction, XOR, XNOR, AND and or function. **(08 Marks)**

c. Explain Manchester carry chain. **(06 Marks)**

7	a.	Explain the architectural issues related to VLSI subsystem design.	(06 Marks)
	b.	Explain in detail the generic structure of an FPGA.	(08 Marks)
	c.	Explain switch logic of 4-way multiplexer for nMOS switches.	(06 Marks)
8	a.	Explain the following: i) Pseudo-nMOS logic ii) Dynamic CMOS logic	(10 Marks)
	b.	Summarize goals and techniques of FPGA.	(10 Marks)
9	a.	What are timing considerations in system design?	(06 Marks)
	b.	Explain Observability and Controllability in testing.	(06 Marks)
	c.	Explain 3-transistor Dynamic RAM cell with neat diagram.	(08 Marks)
10	a.	Explain nMOS pseudo-static RAM cell with schematic diagram.	(10 Marks)
	b.	Explain the following: i) BIST ii) Adhoc Testing.	(10 Marks)

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