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10EC751

Seventh Semester B.E. Degree Examination, July/August 2021
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. What is Digital signal processing? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail. **(06 Marks)**

b. The sequence x(n) = [0, 3, 6, 9] is interpolated using interpolation sequence $b_k = \left[\frac{1}{3}, \frac{2}{3}, 1, \frac{2}{3}, \frac{1}{3}\right]$ and the interpolation factor of 3. Find the interpolated sequence y(m). **(08 Marks)**

c. For the FIR filter $y(n) = \frac{x(n) + x(n-1) + x(n-2)}{3}$, determine the

i) System function
ii) Magnitude response
iii) Phase response
iv) Group delay. **(06 Marks)**

2 a. Implement a 4 bit shift right barrel shifter; tabulate the output for different bit shift. **(06 Marks)**

b. Give the structure of a 4×4 Braun multiplier, explain its concept. What modification is required to carry out multiplication of signed numbers and comment on speed? **(08 Marks)**

c. Explain circular addressing mode with the help of algorithm. **(06 Marks)**

3 a. List the architectural features of three fixed point DSPs. **(06 Marks)**

b. Explain the addressing modes of TMS320C54XX processor. Give example. **(12 Marks)**

c. Assume that the current contents of AR3 to be 400h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the current contents of AR0 are 40h i) *AR3+0 B ii) *AR3 – 0 B. **(02 Marks)**

4 a. Explain the instruction of TMS320C54XX MPY, MAC, MAS with examples. **(06 Marks)**

b. Write a program in TMS320C54XX to compute y(n) = h(0)x(n)+h(1) x(n – 1) +h(2)x(n – 2) using the MAC instruction. **(06 Marks)**

c. Show the pipeline operation of the following sequence of instructions if the initial values of AR1, AR3, A are 84, 81, 1 and the values stored in memory locations, 81, 82, 83, 84 are 2, 3, 4, 6. Also provide the values of registers AR3, AR1, T and accumulator, A after completion of each cycle.

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ADD  *AR3+, A
LD   *AR1+, T
MPY  *AR3+, B
ADD B, A
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(08 Marks)

5 a. Explain the Q-notation to multiply two Q_{15} number to produce Q_{15} number result, and also write a program for TMS320C54XX to multiply numbers representing Q numbers. **(06 Marks)**

b. What is the drawback of using linear interpolation for implementing interpolation filter? Explain a scheme that overcomes this drawback. **(06 Marks)**

c. Determine the value of each of the following 16bit number represented using the given Q notation

i) 4400h as Q_0 and Q_7

ii) ·3125 as Q_{15}

iii) –·1958 as Q_{15}

iv) 136 as Q_7 **(08 Marks)**

6 a. Write an ALP for implementing following on TMS320C54XX processors

i) Bit reversed address generation

ii) Spectrum of the transformed data. **(08 Marks)**

b. Derive the equation to implement a butterfly structure in DIT-FFT algorithm and explain how scaling prevents overflow condition in the same. **(08 Marks)**

c. What minimum size FFT must be used to compute 500 points DFT? And also determine the number of stages required for FFT, number of butterflies in each stage and the total number of butterflies needed for the entire computation. **(04 Marks)**

7 a. What are interrupts? How interrupts are handled by the TMS320C54XX DSP processor with flow chart. **(08 Marks)**

b. How does DMA help in increasing the speed of DSP processors and also explain register sub addressing technique for configuring DMA. **(08 Marks)**

c. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor. Use 2K × 8 SRAM chip. **(04 Marks)**

8 a. Explain JPEG encoding and decoding with the help of block diagram. **(10 Marks)**

b. With the help of neat block diagram, explain PCM3002 codes. **(10 Marks)**

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