

CBCS SCHEME

18MCA15

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First Semester MCA Degree Examination, Dec.2019/Jan.2020 Computer Organization

Time: 3 hrs.

Max. Marks: 100

Note: Answer FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Solve the following numbers in to Equivalent values (10 Marks)
- i) $DAD_{(16)} = (?)_{10}$
 - ii) $A35.B_{(16)} = (?)_8$
 - iii) $101101011.1110_{(2)} = (?)_{16}$
 - iv) $623.77_{(8)} = (?)_{(16)}$
 - v) $4096.3125_{(10)} = (?)_{(2)}$
- b. Compute the steps in Performing $(r - 1)$'s Complement of Subtraction and solve the following : $M = 1000100$ $N = 1010100$ (10 Marks)

OR

- 2 a. Label the Basic theorems and Properties of Boolean Algebra along with the Axiomatic definition of Boolean Algebra State and Prove DeMorgan's Law. (10 Marks)
- b. Compute the following from POS to SOP $F = X(Y + Z)$ $(X + Y + Z)$ and Interpret $F(A, B, C, D) = \sum(1, 3, 5, 7, 9) + D(6, 12, 13)$. Using K-Map. (10 Marks)

Module-2

- 3 a. Describe Basic Logic gates. Define universal gates. State and Describe NAND and NOR as Universal gates. (10 Marks)
- b. Construct a 4-bit Decimal Adder using Binary Coded Decimal Logic. (10 Marks)

OR

- 4 a. Illustrate the Decoder and Encoder with Truth Table and circuit diagram. (10 Marks)
- b. Explain Booth algorithm with the following example $5 * -3$. Using 4-Bit numbers. (10 Marks)

Module-3

- 5 a. Define Computer. Label the different characteristics of a computer with the different types. And describe the Functional units of a computer. (10 Marks)
- b. Describe the interprocess Communication between CPU and Memory. (05 Marks)
- c. Outline Single Bus Structure and Two Bus Structure with block diagram. (05 Marks)

OR

- 6 a. Define Addressing modes, and Describe different Addressing modes with example. (10 Marks)
- b. Classify straight line Sequencing and Branching with an example program to find Sum of Array Elements. (10 Marks)

Module-4

- 7 a. Explain the different types of Interrupts. Describe Interrupt Hardware. (10 Marks)
- b. Describe how Interrupts can be handled? And also explain the methods of controlling Interrupts. (10 Marks)

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OR

- 8 a. Illustrate the I/O Techniques in which CPU is not Continuously involved in Data Transfer. (10 Marks)
b. Analyze the Different approaches to Bus Arbitration. (10 Marks)

Module-5

- 9 a. Design DRAM with neat diagram, Explain internal organization of asynchronous dynamic memory chip. (10 Marks)
b. Explain the working of Cache memory along with Direct Mapping Technique. (10 Marks)

OR

- 10 Write short notes on:
a. Virtual Memory
b. ROM Cell
c. CISC and RISC
d. BIG – ENDIAN and LITTLE – ENDIAN. (20 Marks)
