CMR
INSTITUTE OF
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Internal Assesment Test - III

Sub:	Analog Circuits							Code:	18EC42
Date:	29/ 07/ 2021	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	ECE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1.	Explain a Class B Output stage. Prove that the maximum conversion efficiency of a Class B transformer coupled amplifier is 78.5%.	[10]	CO3	L3
2.	Explain with a neat diagram and relevant expressions, an opamp voltage series feedback amplifier	[10]	CO4	L3
3.	(a)Explain the basic comparator circuit using an opamp. How can this circuit be used in an application as a zero crossing detector?	[06]	CO4	L3
	(b) What is cross over distortion?	[04]	CO3	L3
4.	Explain an Instrumentation amplifier using transducer bridge with relevant equations	[10]	CO4	L3
5.	Explain the operation of a Successive –approximation ADC with neat circuit diagram.	[10]	CO5	L3
6.	Explain the operation of 4-bit R-2R DAC with neat circuit. For the R-2R DAC, with R=10kΩ and R_F=20kΩ and V_{REF}=5V, determine the output voltage when the inputs b0=b1=5V and b2=b3=0V	[10]	CO5	L3
7.	Discuss about summing, scaling and averaging amplifier for inverting configuration	[10]	CO4	L3
8.	For an opamp non-inverting amplifier using 741 IC with R_L=1 KΩ and R_F=10KΩ, A= 200,000; Ri =2MΩ, Ro = 75Ω, fo =5 Hz; supply voltages ±15V, output voltage swing = ±13V, Compute A_F, R_{if}, R_{of}, f_F.	[10]	CO4	L3

Analog Circuits (18EC42)_IAT-3

Marking Scheme-4th Sem

Exam Date: 29, July_2021

Q-1 Class B explanation -5 marks

Efficiency calculation- 5 marks

Q-2 Diagram-2 marks

Explanation-8 marks

Q-3 (a)Explanation-3 marks

Application- 3 marks

(b) Expalnation-4 marks

Q-4 Circuit- 2 marks

Explanation-6 marks

Equations-32 marks

Q-5 Circuit-4 marks

Explanation-6 marks

Q-6 Explanation-6 marks

Numericals- 4 marks

Q-7 Summing-4 marks, Scaling-3 marks, Averaging-3 marks

Q-8 Diagram-2 marks, Af, Rif, Rof, Ff (2 mark each)

29-07-21

ANALOG CIRCUITS - 18EC42

IAT-3

Ans 8 $R_L = 1K\Omega$ and $R_F = 10K\Omega$

$A = 200,000$, $R_i = 2M\Omega$, $R_o = 75\Omega$, $f_o = 5Hz$

supply voltages $= \pm 15V$

output voltage swing $= \pm 13V$

to find B: $B = \frac{R_L}{R_L + R_F} = \frac{1k\Omega}{1k\Omega + 10k\Omega} = \frac{1}{11} k\Omega$

$$1 + AB = 1 + \frac{200000}{11} = 1 + 18181.818 = 18182.8$$

i) To find A_F : $A_F = \frac{A}{1+AB} = \frac{200000}{18182.8} = 10.9994$

$\therefore A_F = 10.999$

ii) To find R_{iF} : $R_{iF} = R_i(1+AB) = 2M\Omega(18182.8) = 2\times10^6(18182.8)$

$= 3.6365 \times 10^{10}$

$\therefore R_{iF} = 3.637 \times 10^{10}\Omega$

iii) To find R_{of} : $\frac{R_o}{1+AB} = R_{of} \Rightarrow R_{of} = \frac{75}{18182.8} = 4.1247 \times 10^{-3}\Omega$

$\therefore R_{of} = 4.124 m\Omega$

iv) To find f_F : $f_F = f_o \times (1+AB)$

$= 5 \times (18182.8) = 90914 Hz$

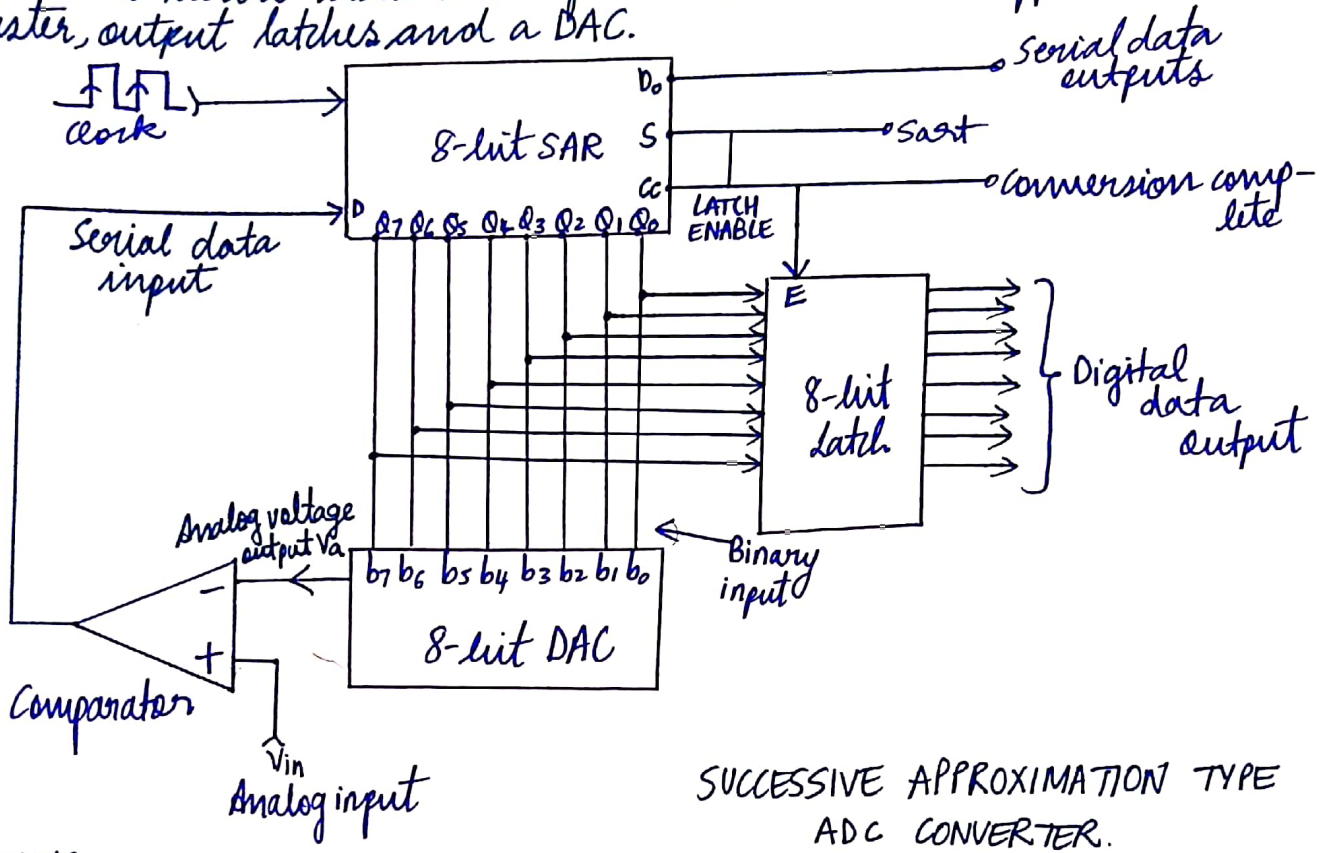
$= 90.914 kHz$

$\therefore f_F = 90.914 kHz$

Ans 5

SUCCESSIVE-APPROXIMATION ADC: It converts an analog voltage to digital output that best represents the input. They are also specified as 8, 10, 12, 16, etc bit.

The circuit below uses a comparator, a successive approximation register, output latches and a DAC.



SUCCESSIVE APPROXIMATION TYPE ADC CONVERTER.

WORKING:

→ At the start of a conversion cycle, the SAR is reset by holding the start (S) signal high.

→ On the LOW to HIGH transition, the most significant output bit Q_7 of the SAR is set

→ The DA converter then generates an analog equivalent to the Q_7 bit, which is compared with V_{in}.

→ If the comparator output is low, that means DAC output > V_{in} and the SAR will clear its MSB Q_7. On the other hand, if comparator output is high, which means DAC output < V_{in}, the SAR will keep MSB Q_7 set.

→ Similarly depending on the comparator output, the SAR will then either keep or reset bit Q_6, on the next clock pulse LOW to HIGH.

→ This process is continued until the SAR tries all the bits (i.e Q_5,

Q_4, Q_3, Q_2, Q_1, Q_0)

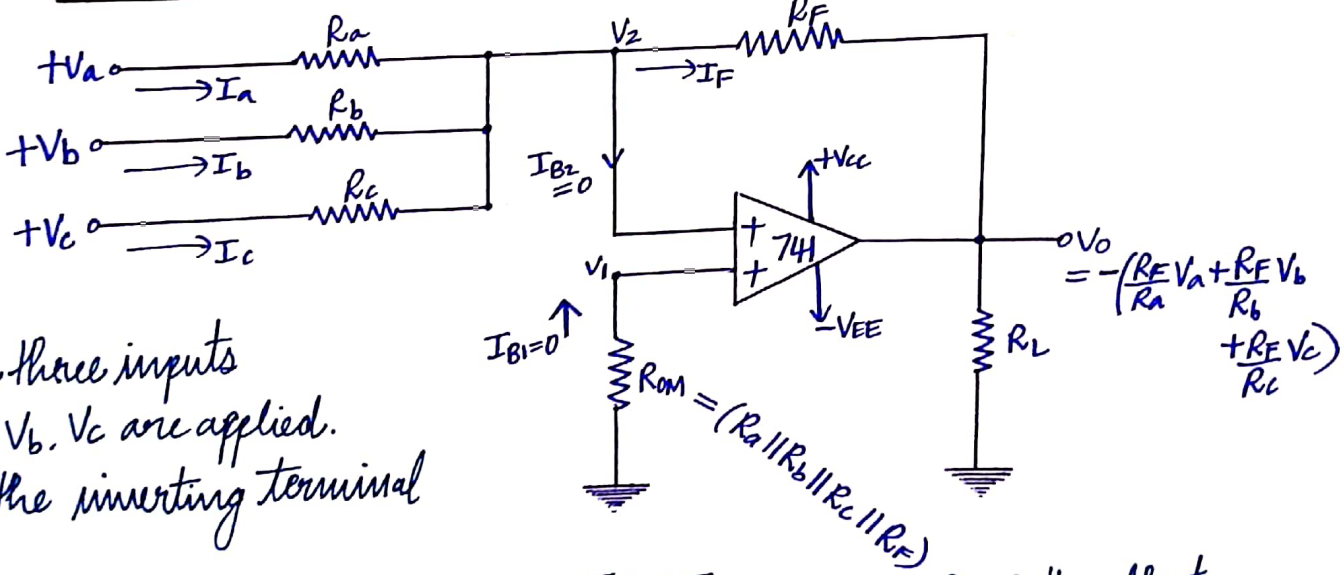
→ As soon as LSB Q_0 is tried, the SAR forces the conversion complete (CC) signal HIGH to indicate that the parallel output lines contains valid data.

→ The CC signal in turn enables the latch and digital data appears at the output of the latch, which gives the digital representation of the analog voltage V_{in}.

→ For 8 bit SAR type ADC eight clock pulse is required, for 12 bit, 12 clock pulse is required and so on.

→ The advantages are that it has high speed and a very good resolution.

Ans 7: INVERTING CONFIGURATION:



The three inputs V_a, V_b, V_c are applied at the inverting terminal

FIGURE

R_{OM} is the offset minimizing resistor

Apply KCL at node V_2 : $I_a + I_b + I_c = I_B + I_F$

$I_B = 0$ for ideal OP-AMP.

$\therefore I_a + I_b + I_c = I_F$

$$\Rightarrow \frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_c - V_2}{R_c} = \frac{V_2 - V_o}{R_F}$$

($V_1 = V_2$ for ideal op-amp)

$$\therefore \frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

$$\therefore V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right) \quad \text{---(1)}$$

SUMMING AMPLIFIER: In the figure, if $R_a = R_b = R_c = R$, then Eq.(1) can be written as $V_o = -\frac{R_F}{R}(V_a + V_b + V_c)$

and if R is choosen such that $R = R_F$

$$V_o = -(V_a + V_b + V_c)$$

It is clear that output voltage is equal to the negative sum of all input voltages.

SCALING OR WEIGHTED AMPLIFIER: If each input voltage is amplified by different factor, it is known as scaling amplifier. This condition can be accomplished if R_a, R_b and R_c are different in values.

$$\therefore V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

where $\frac{R_F}{R_a} \neq \frac{R_F}{R_b} \neq \frac{R_F}{R_c}$

AVERAGING CIRCUIT: To convert it to an averaging circuit, we should have $R_a = R_b = R_c = R$.

Also, the gain by which each input is amplified must be equal to 1 or over number of inputs (n).

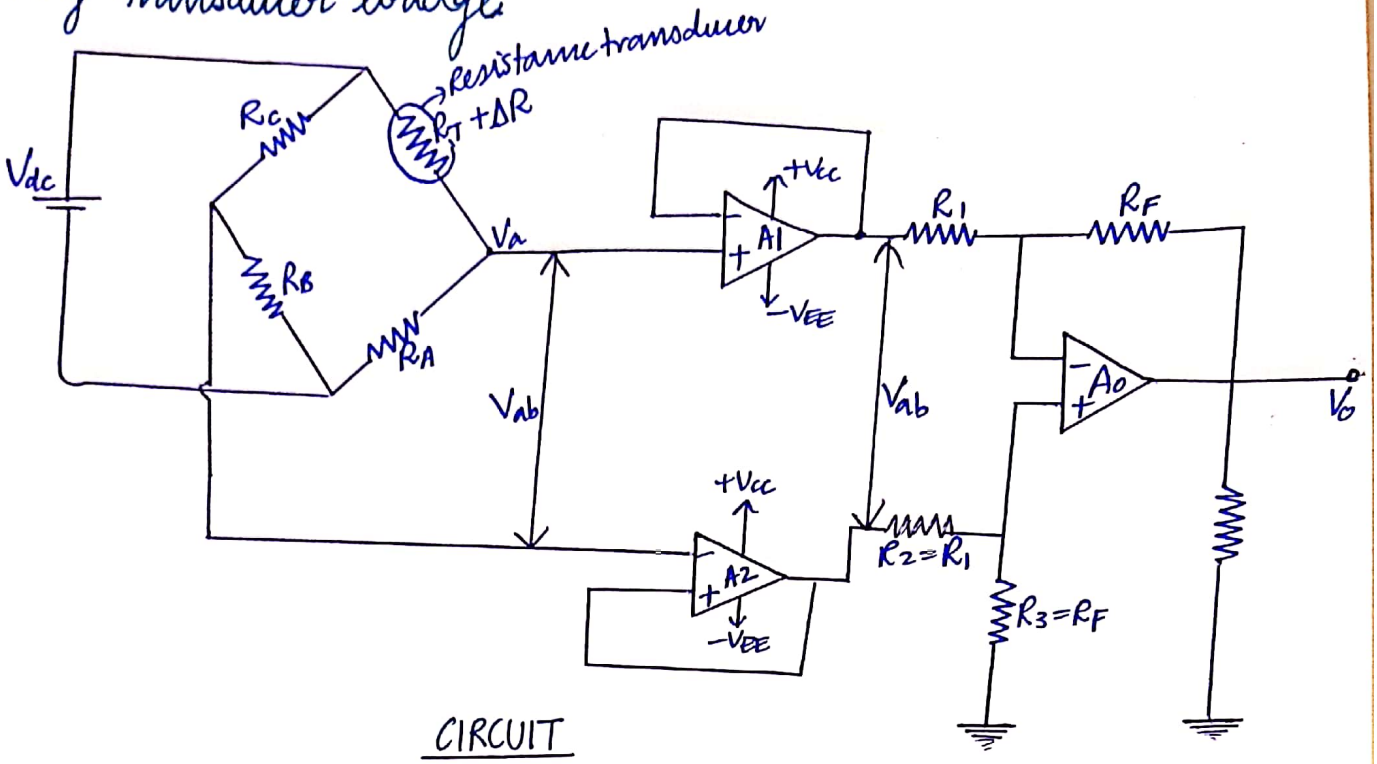
$$\frac{R_F}{R} = \frac{1}{n} = \frac{1}{3}$$

$\therefore$ output voltage $V_o = -\left(\frac{V_a + V_b + V_c}{3}\right)$

↳ This is the negated average of three inputs.

Ans 4: **INSTRUMENTATION AMPLIFIER:** It is intended for precise, low-level signal amplification where low noise, low thermal and time drifts, high input resistance and accurate closed loop gain are required.

In the figure, a simplified differential instrumentation amplifier using transducer bridge.



CIRCUIT

→ Resistors R_A, R_B, R_C and R_T are in balanced condition, $\frac{R_C}{R_B} = \frac{R_T}{R_A}$

At this condition $V_a = V_b$

But whenever there is change in resistance of transducer R_T, then $V_a \neq V_b$. Let the change in the resistance to R_T be ΔR.

$$\therefore V_a = V_{dc}\left(\frac{R_A}{R_A + (R_T + \Delta R)}\right) \text{ and } V_b = V_{dc} \cdot \left(\frac{R_B}{R_B + R_C}\right)$$

$$\therefore V_{ab} = V_a - V_b = V_{dc}\left(\frac{R_A}{R_A + (R_T + \Delta R)}\right) - V_{dc}\left(\frac{R_B}{R_B + R_C}\right)$$

→ If $R_A = R_B = R_C = R_T = R$, then $V_{ab} = V_{dc}\left(\frac{\Delta R}{2(2R + \Delta R)}\right)$

→ The output voltage V_{ab} of the bridge is then applied to the differential instrumentation amplifier consisting of three OPAMPS A1, A2, A3

→ The voltage follower A1 and A2 help in eliminating loading of the bridge circuit. Now, the third amplifier A3, having gain $\left(-\frac{R_F}{R_1}\right)$, comes into picture to amplify V_{ab}, so the output V_o, can be given as,

$$V_o = \left(\frac{-R_F}{R_1}\right) V_{ab} = \frac{(\Delta R)\, V_{dc}}{2(2R+\Delta R)} \cdot \frac{R_F}{R_1}$$

$\therefore \Delta R$ is very small, so, $2R + \Delta R \approx 2R$, $\therefore V_o = \frac{R_F}{R_1} \cdot \frac{\Delta R}{4R} V_{dc}$

→ The equation indicates that V_o is directly proportional to the change in resistance ΔR of the transducer R_T
It can be thermister.

→ Some commonly used Instrument amplifiers are MA7425, LH0036 etc.

Ans 1: CLASS B OUTPUT STAGE:

→ It consists of complementary pair of transistor (an pnp and npn)
→ They are connected such that both cannot conduct simultaneously

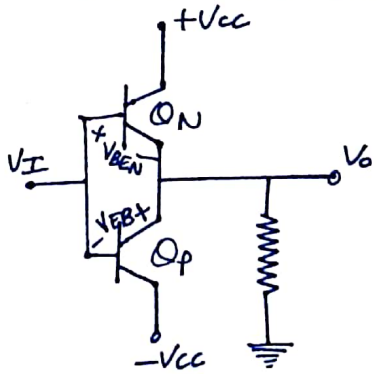
CIRCUIT OPERATION:

CASE ①: ($V_I = 0$) → Both Q_N and Q_P in cut off ($V_o = 0$)

CASE ②: Q_N conducts (operates as emitter follower)
↓ $V_I = +ve$, $V_I > 0.5V$
$V_o = V_I - V_{BEN}$ (output follows V_I). Thus, Q_N supplies load current.
Meanwhile, emitter base junction of Q_P will be reverse biased by V_{BE} of Q_N (approx 0.7V). and Q_P is cut off.

CASE ③: ($V_I = -ve$) and ($V_I < -0.5V$)

Class B output stage



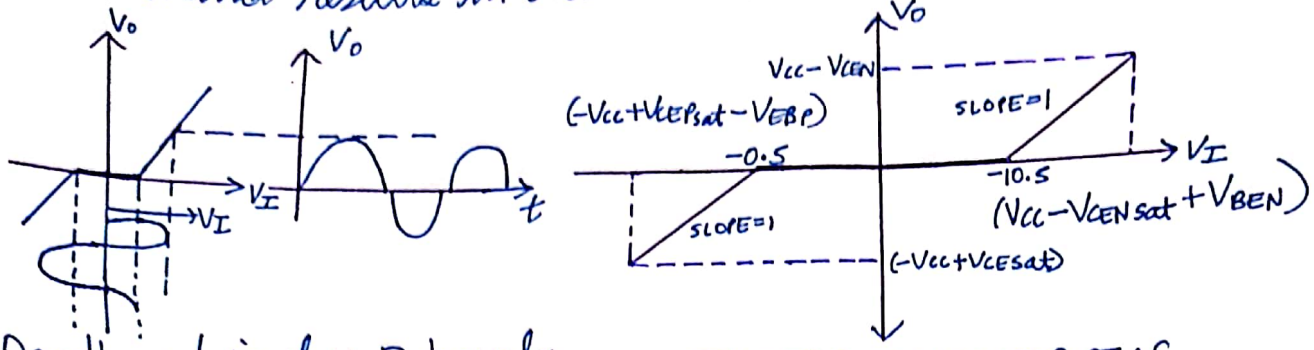
→ Q_P is on and gets used as emitter follower.
→ $V_o = V_I + V_{EBP}$ (output follows V_I)
→ Q_P supplies the load current but Q_N is off
The circuit operates in push pull fashion as Q_N pushes (source) current into the load when V_I is present and Q_P pulls (sinks) current from the load when V_I is negative.

TRANSFER CHARACTERISTICS:

Both transistors are off in a range of V_I centred around zero and

So $V_o = 0$

This deadband results in crossover distortion.



Deadband in class B transfer characteristics resulting in cross-over distortion.

TRANSFER CHARACTERISTICS

→ The effect of crossover distortion will be most pronounced when input signal amplitude is small.

→ The distortion in audio power amplifiers gives unpleasant sounds

POWER CONVERSION EFFICIENCY:

→ Neglect crossover distortion and let output sinusoidal have peak amplitude of V_o.

→ Average load power is $P_L = \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{R_L} = \frac{\hat{V}_o^2}{2R_L}$

→ Average power drawn from each of the two power supplies, $P_{S^+} = P_{S^-} = (I_{avg})V_{cc}$

→ $P_{S^+} = P_{S^-} = \left(\frac{\hat{V}_o}{\pi R_L}\right)V_{cc} \rightarrow I_{avg.} = \frac{I_m}{\pi} = \frac{\hat{V}_o}{R_L \pi}$

→ P_S (total power supply) $= P_{S^+} + P_{S^-} \Rightarrow P_S = \frac{2\hat{V}_o}{\pi R_L} V_{cc}$

→ Efficiency $(\eta) = \frac{P_L}{P_S} = \frac{\left(\frac{\hat{V}_o^2}{2R_L}\right)}{\left(\frac{2\hat{V}_o}{\pi R_L}\right)V_{cc}} = \frac{\pi \hat{V}_o}{4V_{cc}}$

→ When $\hat{V}_o$ is max, i.e, $V_{cc} \Rightarrow \boxed{\eta\% = \frac{\pi}{4} = 78.5\%}$

Also, max average load power, $P_{L\,max} = \frac{V_{cc}^2}{2R_L}$

(When $\hat{V}_o = V_{cc}$)