CBCS SCHEME

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17EC53

Fifth Semester B.E. Degree Examination, Feb./Mar.2022
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the emergence of Hardware Description Languages (HDLs). **(05 Marks)**

b. Explain different levels of abstraction used to describe a module in verilog. **(10 Marks)**

c. Write a note on popularity of Verilog HDL. **(05 Marks)**

OR

2 a. Explain the typical design flow for designing VLSI IC. **(08 Marks)**

b. Explain the top-down design methodology with an example of 4-Bit Parallel adder. **(07 Marks)**

c. What are instances and instantiation? Illustrate with an example. **(05 Marks)**

Module-2

3 a. Explain the following with suitable example :

(i) Comments.
(ii) Sized and Unsized numbers.
(iii) Strings.
(iv) Identifiers & Keywords.
(v) Escaped identifiers. **(10 Marks)**

b. A 4 : 1 multiplexer has I/O ports shown in the figure Q3 (b). Write module definition by name "mux_4_1" including portlist and its declaration. Declare a top-level module "stimulus" and instantiate module "mux_4_1" in it. Connect the ports by name. (No need to show internals). Write verilog code for the above. **(06 Marks)**

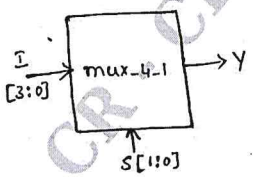

Fig. Q3 (b)

c. Explain the port connection rules. **(04 Marks)**

OR

4 a. Explain the following with suitable example :

(i) Integer.
(ii) 2-Dimensional arrays.
(iii) Variable vector part select.
(iv) Vector part select.
(v) Parameter. **(10 Marks)**

b. Explain the components of a verilog module. **(05 Marks)**

c. Write a Verilog description for a SR latch and its stimulus by considering all possible I/P combinations. **(05 Marks)**

Module-3

5 a. Write a verilog description for the circuit shown in Fig. Q5 (a) using gate level abstraction. The delay specification of these gates are given in Table Q5 (a). Also write stimulus in verilog. **(10 Marks)**

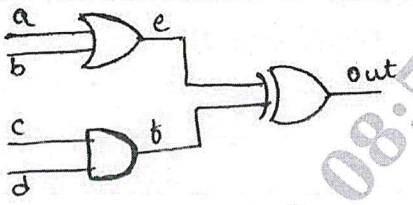

Fig. Q5 (a)

Delay	Min	Max	Typical
Rise	1	3	2
Fall	3	5	4
Turn off	5	7	6

Table Q5 (a)

b. Explain the following with an example:
(i) Logical AND operator. (ii) Modulus operator.
(iii) Case equality operator. (iv) Reduction OR operator.
(v) Concatination operator. **(10 Marks)**

OR

6 a. Write a description for 2 : 4 decoder using conditional operator. Note use regular assignment delay of 5 time units. Also write stimulus for all possible I/P combinations. **(08 Marks)**

b. Implement a 4 bit magnitude comparator using data flow level of abstraction. Comparator has 2 four bit inputs A and B and 3 one bit outputs A_gt_B, A_lt_B and A_eq_B. The logical equations are as follows:

$$A\_gt\_B = A(3)\cdot\overline{B(3)} + x(3)\cdot A(2)\cdot\overline{B(2)} + x(3)\cdot x(2)\cdot A(1)\cdot\overline{B(1)} + x(3)\cdot x(2)\cdot x(1)\cdot A(0)\cdot\overline{B(0)}$$

$$A\_lt\_B = \overline{A(3)}\cdot B(3) + x(3)\cdot\overline{A(2)}\cdot B(2) + x(3)\cdot x(2)\cdot\overline{A(1)}\cdot B(1) + x(3)\cdot x(2)\cdot x(1)\cdot\overline{A(0)}\cdot B(0)$$

$$A\_eq\_B = x(3)\cdot x(2)\cdot x(1)\cdot x(0)$$

where $x(i) = A(i)\cdot B(i) + \overline{A(i)}\cdot\overline{B(i)}$

Also write stimulus for few combinations of A and B. **(12 Marks)**

Module-4

7 a. Explain event based time control with suitable example. **(12 Marks)**

b. Write a verilog description for 4 : 2 priority encoder using casex statement. **(04 Marks)**

c. Explain Repeat loop with an example. **(04 Marks)**

OR

8 a. Explain sequential and parallel blocks with example. **(10 Marks)**

b. Write a verilog description for 4-bit BCD upcounter and also write its stimulus. **(10 Marks)**

Module-5

9 a. Explain the following :
(i) Design synthesis (ii) Design optimization.
(iii) Design fitting. **(12 Marks)**

b. Write a VHDL description for full adder using two half adders. Also write VHDL description for half adder. **(08 Marks)**

OR

10 a. Explain the following data types with examples:
(i) Enumerate (ii) Physical (iii) Array **(12 Marks)**

b. Write a VHDL description for 3 : 8 decoder using data flow architecture. **(08 Marks)**

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