

Time 3 hrs

18EC56

Fifth Semester B.E. Degree Examination, Feb./Mar. 2022
Verilog HDL

Max. Marks: 100

		Note: Answer any FIVE full questions, choosing ONE full question from each module.		
olank pages. 50, will be treated as malpractice.			Module-1	
rac	1	a.	Explain a typical design flow for designing VLSI IC circuits using the block di	agram.
nalp		α.	Explain a typical design no water designing visit to enouse using and one of	(10 Marks)
as n		b.	Explain the importance of HDLs.	(05 Marks)
ted		c.	Explain the trends in HDLs.	(05 Marks)
trea			The state of the s	
be be			OR *	
pag will	2	a.	Explain the different levels of abstraction used for programming in verilog.	(08 Marks)
lank 50, 1	_	b.	Write the verilog code for 4-bit ripple carry counter. Also write the stimulus.	(12 Marks)
50 11		٠.		
inin 2+8			Module-2	
ma g, 4	3	a.	Explain the components of verilog module with block diagram.	(06 Marks)
e re		b.	Explain the following data types with an example in verilog.	
n th ritte		0,	i) Registers ii) Arrays iii) Parameters iv) Nets v) Integers.	(10 Marks)
es o		c.	Explain the port connection rules in verilog.	(04 Marks)
lin		•		
oss			OR ()	
al cı	4	a.	Write the verliog description of SR latch. Also write stimulus code.	(10 Marks)
log log	7	b.	Explain \$display, \$monitor, \$finish and \$stop system tasks with examples.	(10 Marks)
diag or an		0.	Explain dataplay, different and dataplay and analysis	(
aw			Module-3	
y dr	5	а	What are rise, fall and turn off delays? How they are specified in verilog?	(06 Marks)
oril to e	5	b.	What would be the output of the following for $A = 4^{\circ}b0111$ and $B = 4^{\circ}b1001$.	(100,000,000,000,000,000,000,000,000,000
ouls		0.	i) &B ii) A<<2 iii) $\{A, B\}$ iv) $\{2\{B\}\}$ v) $A^{A}B$ vi) $A B$ vii) $A*B$ viii) $A < B$. (08 Marks)
omp		c.	Mention the symbol, truth table and an example for BUFIF1 and BUFIF0 prim	itive gates
s, co		0.	Mention the symbol, truth capte and an example for Both 1 and Both opinin	(06 Marks)
wer				(0000000)
ans ntif		T.	OR	
On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Any revealing of identification, appeal to evaluator and /or equations written eg, $42+8=50$, will be	6	a.	Design AOI based 4 to 1 multiplexer and write the verilog description and its st	imulus.
ig y	U	u.	A de la companya de l	(10 Marks)
letir ding		b.	Write the verilog data flow description for 4-bit full adder with carry look -ahe	ad logic.
mp			are resident and a second and a	(10 Marks)
0 CO				
171			Module-4	
Important Note : 1. 2.	7	a.	Explain blocking and non-blocking assignments with an example.	(10 Marks)
lote		b.	Write a verilog code for clock generation with a period of 20 units using foreve	
Z Ta				(05 Marks)
orta		c.	Write the differences between the tasks and functions.	(05 Marks)
du		100	Winds of the state	
_			OR	(10 84 1-1
	8	a.	Discuss sequential and parallel blocks with examples.	(10 Marks)
		b.	Write a verilog program for 8:1 multiplexer using case statement.	(10 Marks)
			1 of 2	

Module-5

9 a. Write the verilog description for D - flipflop using assign and deassign procedural continuous assignments. (10 Marks)

b. Explain defparam statement with an example.

(10 Marks)

OR

10 a. What is logic synthesis? Explain the flow diagram for the designer's mind as the logic synthesis tool. (10 Marks)

b. What will be the following statements translate to when run on a logic synthesis tool:

Assign $\{C\text{-out}, \text{sum}\} = a + b + C \text{ in };$

Assign out = (s) ? i1 : i0;

(10 Marks)

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2 of 2