

CBCS SCHEME



Fifth Semester B.E. Degree Examination, Feb./Mar. 2022

Verilog HDL

18EC56

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain a typical design flow for designing VLSI IC circuits using the block diagram. (10 Marks)
- b. Explain the importance of HDLs. (05 Marks)
- c. Explain the trends in HDLs. (05 Marks)

OR

- 2 a. Explain the different levels of abstraction used for programming in verilog. (08 Marks)
- b. Write the verilog code for 4-bit ripple carry counter. Also write the stimulus. (12 Marks)

Module-2

- 3 a. Explain the components of verilog module with block diagram. (06 Marks)
- b. Explain the following data types with an example in verilog.
i) Registers ii) Arrays iii) Parameters iv) Nets v) Integers. (10 Marks)
- c. Explain the port connection rules in verilog. (04 Marks)

OR

- 4 a. Write the verilog description of SR latch. Also write stimulus code. (10 Marks)
- b. Explain \$display, \$monitor, \$finish and \$stop system tasks with examples. (10 Marks)

Module-3

- 5 a. What are rise, fall and turn off delays? How they are specified in verilog? (06 Marks)
- b. What would be the output of the following for $A = 4'b0111$ and $B = 4'b1001$.
i) $\&B$ ii) $A \lll 2$ iii) $\{A, B\}$ iv) $\{2\{B\}\}$ v) $A \wedge B$ vi) $A \parallel B$ vii) $A * B$ viii) $A \leq B$. (08 Marks)
- c. Mention the symbol, truth table and an example for BUFIF1 and BUFIF0 primitive gates. (06 Marks)

OR

- 6 a. Design AOI based 4 to 1 multiplexer and write the verilog description and its stimulus. (10 Marks)
- b. Write the verilog data flow description for 4-bit full adder with carry look-ahead logic. (10 Marks)

Module-4

- 7 a. Explain blocking and non-blocking assignments with an example. (10 Marks)
- b. Write a verilog code for clock generation with a period of 20 units using forever loop. (05 Marks)
- c. Write the differences between the tasks and functions. (05 Marks)

OR

- 8 a. Discuss sequential and parallel blocks with examples. (10 Marks)
- b. Write a verilog program for 8 : 1 multiplexer using case statement. (10 Marks)

Module-5

- 9 a. Write the verilog description for D – flipflop using assign and deassign procedural continuous assignments. (10 Marks)
- b. Explain defparam statement with an example. (10 Marks)

OR

- 10 a. What is logic synthesis? Explain the flow diagram for the designer's mind as the logic synthesis tool. (10 Marks)
- b. What will be the following statements translate to when run on a logic synthesis tool :
Assign {C-out, sum } = a + b + C in ;
Assign out = (s) ? i1 : i0 ; (10 Marks)

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