CBCS SCHEME

USN | | | | | | | | | | 15EC53

Fifth Semester B.E. Degree Examination, Feb./Mar. 2022
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain design and stimulus block of Ripple carry counter (4 bit). (08 Marks)
b. Explain typical design flow for designing VLSI IC circuits. (08 Marks)

OR

2 a. Explain evolution of computer aided design and importance of HDLs. (08 Marks)
b. Explain modulus and instances with example. (08 Marks)

Module-2

3 a. Explain nets and register data types of verilog HDL. (08 Marks)
b. Explain system tasks and compiler directives of verilog HDL. (08 Marks)

OR

4 a. Explain components of a verilog module and write verilog description for SR Latch. (08 Marks)
b. Explain port connection rules in verilog HDL and explain connection by ordered list method of making connection with example. (08 Marks)

Module-3

5 a. Explain gate types supported by verilog HDL. (08 Marks)
b. Write verilog description of multiplexer and 1 bit full subtractor. (08 Marks)

OR

6 a. Explain gate delays with example. (08 Marks)
b. Explain operator types of verilog HDL. (08 Marks)

Module-4

7 a. Explain initial and always statement with verilog description. (08 Marks)
b. Explain delay based timing control and event based timing control. (08 Marks)

OR

8 a. Explain different types of looping statements of verilog HDL. (08 Marks)
b. Explain sequential and parallel blocks with example. (08 Marks)

Module-5

9 a. Explain entity and architecture declaration in VHDL. (08 Marks)
b. Explain design tool flow diagram in VHDL. (08 Marks)

OR

10 a. Write behavioral, dataflow and structural description of 4 bit equality comparator. (08 Marks)
b. Explain data types, identifiers and attributes of VHDL. (08 Marks)

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