15EC53

Fifth Semester B.E. Degree Examination, Feb./Mar. 2022 Verilog HDL

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.			
Module-1			
1	a.	Explain design and stimulus block of Ripple carry counter (4 bit).	(08 Marks)
•	b.	Explain typical design flow for designing VLSI IC circuits.	(08 Marks)
		OR	
2	a.	Explain evolution of computer aided design and importance of HDLs.	(08 Marks)
	b.	Explain modulus and instances with example.	(08 Marks)
2	_	Module-2 Evalein note on dissociator data types of words a UDI	(00 Morks)
3	a. b.	Explain nets and register data types of verilog HDL. Explain system tasks and compiler directives of verilog HDL.	(08 Marks) (08 Marks)
	υ.	Explain system tasks and compiler directives of vernog Tibe.	(00 Marks)
		OR	
4	a.	Explain components of a verilog module and write verilog description for SR Late	h.
			(08 Marks)
	b.	Explain port connection rules in verilog HDL and explain connection by ordered	
		of making connection with example.	(08 Marks)
~		Module-3	(00 Mayles)
5	a. b.	Explain gate types supported by verilog HDL. Write verilog description of multiplexer and 1 bit full subtractor.	(08 Marks) (08 Marks)
	υ.	Write verifing description of multiplexer and 1 of full subtractor.	(UO Marks)
		OR	
6	a.	Explain gate delays with example.	(08 Marks)
	b.	Explain operator types of verilog HDL.	(08 Marks)
Module-4			
7		Explain initial and always statement with verilog description.	(08 Marks)
	b.	Explain delay based timing control and event based timing control.	(08 Marks)
		OD	
0		Explain different types of looping statements of verilog HDL.	(08 Marks)
8	a. b.	Explain sequential and parallel blocks with example.	(08 Marks)
	υ.	Explain sequential and parametolocks with example.	(00 1/14/165)
Module-5			
9	a.	0.54	(08 Marks)
*	b.	Explain entity and architecture declaration in VHDL. Explain design tool flow diagram in VHDL. CMRIT LIBRARY CMRIT LIBRARY BANGALORE - 560 007	(08 Marks)
		BWA	
		OR	
10	a	Write behavioral, dataflow and structural description of 4 bit equality comparator.	(08 Marks)

Write behavioral, dataflow and structural description of 4 bit equality comparator. (08 Marks) 10 a. Explain data types, identifiers and attributes of VHDL. (08 Marks)

Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.