CBCS SCHEME

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17TE73

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Write all the masks steps of P-well process and draw the CMOS P-well inverter showing V_{DD} and V_{SS} substrate connections. **(10 Marks)**

b. With neat diagrams and relevant expression, explain the cutoff, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds}. **(10 Marks)**

OR

2 a. Write all the mask steps of nMOS process and draw the cross-sectional view of nWell CMOS inverter. **(10 Marks)**

b. Draw the ideal and non-ideal characteristics of MOSFET and bring out the differences between them along with the reasons for those differences. **(10 Marks)**

Module-2

3 a. Write the lambda based design rules for layers, wires and transistors. **(10 Marks)**

b. Calculate the capacitance of the structure shown in Fig Q3(b) with the following data.
Area capacitance value for metal 1 to substrate = 0.3pF × $10^{-4}/\mu m^2$ (0.075 relative value)
Area capacitance value for polysilicon to substrate = 0.4pF × $10^{-4}/\mu m^2$ (0.1 relative value).

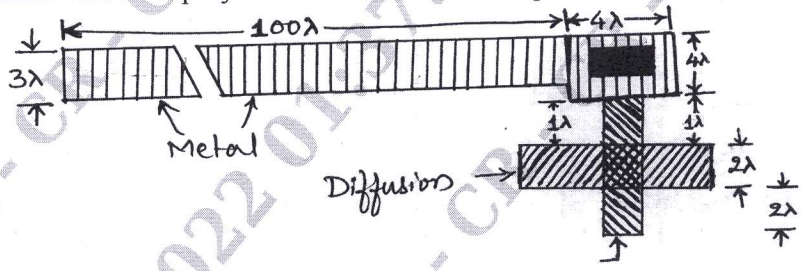

Fig Q3(b) **(10 Marks)**

OR

4 a. Draw the nMOS and CMOS stick diagrams for 2 I/P NAND gate and 2 I/P NOR gate. **(10 Marks)**

b. Calculate the area capacitance of the layer in the Fig Q4(b) for the following criteria.
i) If the layer is metal 1 and relative capacitance is 0.075 □ C_g
ii) If the layer is polysilicon and relative capacitance is 0.1 □ C_g
iii) If the layer is n-type diffusion and relative capacitance is 0.25 □ C_g.

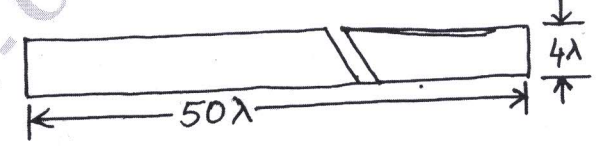

Fig Q4(b) **(10 Marks)**

Module-3

5 a. With relevant diagrams, explain the different basis bus architectures. (10 Marks)
b. With relevant expressions, explain 4-bit carry-look ahead adder. (10 Marks)

OR

6 a. Implement the ALU functions like EX-OR, EX-NOR, AND and OR operations with an adder. Write the block diagram of 2-bit ALU using adder element. (10 Marks)
b. Obtain the Scaling factors for the following parameters.
i) Gate Capacitance (C_g)
ii) Gate Area (A_g)
iii) Maximum operating frequency (f_o)
iv) Power dissipation per gate (P_g)
v) Gate delay (T_d) (10 Marks)

Module-4

7 a. Explain clocked CMOS logic and Pseudo nMOS logic in detail. (10 Marks)
b. With nMOS stick diagram, explain the structured design approach for the implementation of parity generator. (10 Marks)

OR

8 a. Explain Programmable Logic Array (PLA) in detail. (10 Marks)
b. Draw the block diagram of Generic structure of FPGA fabric and explain it. (10 Marks)

Module-5

9 a. Write all the system timing considerations. (10 Marks)
b. Explain three transistor dynamic RAM with neat circuit and stick diagram. (10 Marks)

OR

10 a. With the help of block diagram, explain the process of logic verification. (10 Marks)
b. Write short notes on :
i) Built In Self Test (BIST)
ii) Observability and Controllability. (10 Marks)

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