CBCS SCHEME

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15TE73

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain the behavior of nMOS enhancement mode MOSFET in different regions and draw the V-I characteristics. **(10 Marks)**

b. Explain the following:
i) Channel length modulation
ii) Threshold voltage-body effect. **(06 Marks)**

OR

2 a. Illustrate the nMOS fabrication with neat diagram. **(10 Marks)**

b. Give the comparisons between CMOS and Bipolar Technology. **(06 Marks)**

Module-2

3 a. Obtain the CMOS circuit and stick diagram for the following function $F = \overline{(A + BC)D}$. **(06 Marks)**

b. Using λ-based design rules, draw the layout for a nMOS 3-input NOR gate, using the following transistor L:W ratios:
i) P.U. transistor = 8:1
ii) P.D. transistors = 1:2, 1:2, 1:2 **(10 Marks)**

OR

4 a. For the following structure obtain C_m, C_p, C_g and C_t. Given that the relative values of capacitances are metal 1 = 0.075□C_g, polysilicon = 0.1□C_g. **(08 Marks)**

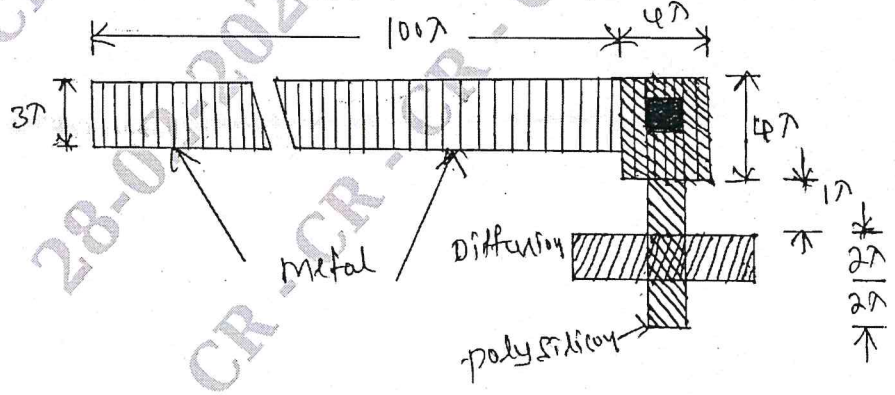

Fig.Q.4(a)

b. Derive the expressions for rise time and fall time delays of a CMOS inverters. What is the condition for symmetrical operation? **(08 Marks)**

Module-3

5 a. Derive scaling factors for the following MOS parameters:
i) Carrier density in channel, Q_{on}
ii) Channel resistance, R_{on}
iii) Gate delay, T_d
iv) Switching energy per gate E_g
Scaling method to be adopted is combined voltage and dimension method. **(08 Marks)**

b. Explain a 4 × 4 barrel shifter with neat diagram. **(08 Marks)**

OR

6 a. How to implement arithmetic and logic operation with a standard adder? Explain with the help of logic expression. **(06 Marks)**

b. Explain carry look ahead adder. **(10 Marks)**

Module-4

7 a. Explain the following:
i) Pseudo nMOS logic
ii) C^2 MOS logic. **(06 Marks)**

b. Explain the structured design of a purity generator with necessary blocks and stick diagram. **(10 Marks)**

OR

8 a. Explain generic structure of FPGA with block diagram. **(08 Marks)**

b. Explain placement and routing with respect to FPGA. **(08 Marks)**

Module-5

9 a. Explain with a neat diagram a 3 transistor dynamic RAM cell. **(08 Marks)**

b. Explain pseudo static memory cell using circuit diagram. **(08 Marks)**

OR

10 a. Write a short notes on:
i) Built In Self Test (BIST)
ii) Scan design technique. **(08 Marks)**

b. Write a short notes on:
i) Stuck-at-faults
ii) Short circuit and open circuit faults. **(08 Marks)**

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