Internal Assessment Test 1 –**SCHEME and SOLUTIONS**

Sub:	Advanced Computer Architecture					Sub Code:	17CS72	Branch:	CSE
Date:	11/11/21	Duration:	90 mins	Max Marks:	50	Sem / Sec:	VII-D(15/17 scheme)	OBE	

Answer any 5 FIVE FULL Questions

		MARKS	CO	RBT
1	Briefly explain about the evolution of computer architecture with a neat diagram.	[10]	CO1	L2
2	Explain Flynn's Classification of Computer architecture along with neat diagrams.	[10]	CO1	L2
3	Explain UMA Model and COMA Model for shared memory multiprocessor systems, With neat diagram.	[10]	CO1	L2
4	Explain the Bernstein's conditions for parallelism. Detect parallelism in the following code using Bernstein's Conditions. P1: C=D*E P2:M=G+C P3:A=B+C P4:C=L+M P5:G=G/E	[10]	CO1	L3
5	Find total processor clock cycles needed to execute a program. Consider the execution of an object code with 200000 instructions on a 20 MHZ processor. The program consists of four major types of instruction. The instruction mix and number of cycles (CPI) needed for each instruction is given below.	[10]	CO1	L3

No	Instruction type	CPI	Instruction mix
1	Arithmetic and logic	1	68%
2	Load/store with cache hit	2	8%
3	Branch	4	14%
4	Memory reference with cache hit	8	10%

i) Find total number of cycles required to execute the program.
ii) Calculate the CPI when the program is executed on uniprocessor system with above trace results.
iii) Calculate the MIPS rate based on CPI obtained in ii.

6	Explain the architecture of Vector super Computer with a neat diagram	[10]	CO1	L2
7 (a)	What are the factors affecting the scalability of computing systems, briefly explain.	[5]	CO1	L2
(b)	List the performance factors and system attributes that influence the performance of a computing system	[5]	CO1	L2
8	With a neat diagram explain the operational model of SIMD super computer	[10]	CO1	L2

CO PO Mapping

Course Outcomes		Modules covered	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	Understand the different computer architectures and hardware technologies	**1**	0	0	2	2	3	0	0	0	0	0	0	0	0	0	0	3
CO2	Explain need of pipelining along with the methods and implementation details and performance enhancement	**2**	0	3	2	3	3	0	0	0	0	0	0	0	0	2	0	3
CO3	Ability to define the hardware requirements of computer system with complete understanding of the memory..	**3**	0	2	3	3	3	0	0	0	0	0	0	0	0	2	0	3
CO4	Compare and contrast the parallel architectures, Illustrate parallel programming concepts including the parallel languages and compilers	**4,5**	2	3	3	2	3	0	0	0	0	0	0	0	0	2	0	3

COGNITIVE LEVEL	REVISED BLOOMS TAXONOMY KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PROGRAM OUTCOMES (PO), PROGRAM SPECIFIC OUTCOMES (PSO)				CORRELATION LEVELS	
PO1	Engineering knowledge	PO7	Environment and sustainability	0	No Correlation
PO2	Problem analysis	PO8	Ethics	1	Slight/Low
PO3	Design/development of solutions	PO9	Individual and team work	2	Moderate/ Medium
PO4	Conduct investigations of complex problems	PO10	Communication	3	Substantial/ High
PO5	Modern tool usage	PO11	Project management and finance		
PO6	The Engineer and society	PO12	Life-long learning		
PSO1	Develop applications using different stacks of web and programming technologies				
PSO2	Design and develop secure, parallel, distributed, networked, and digital systems				
PSO3	Apply software engineering methods to design, develop, test and manage software systems.				
PSO4	Develop intelligent applications for business and industry				

1 **Briefly explain about the evolution of computer architecture with a neat diagram.**

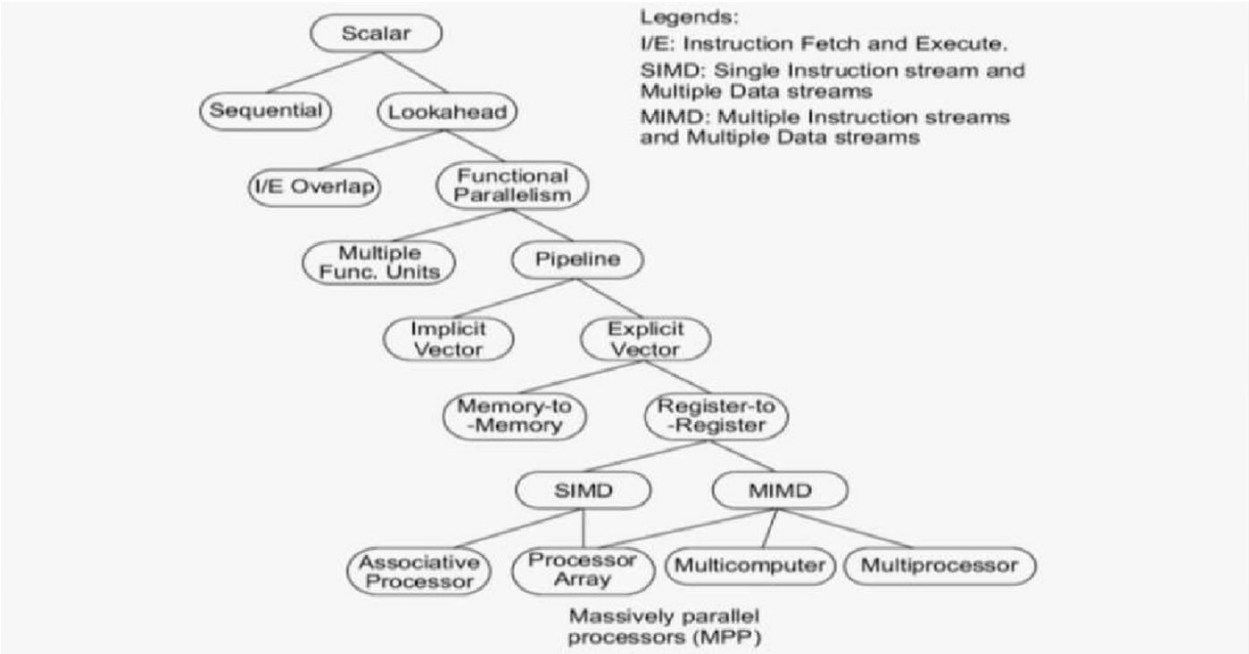
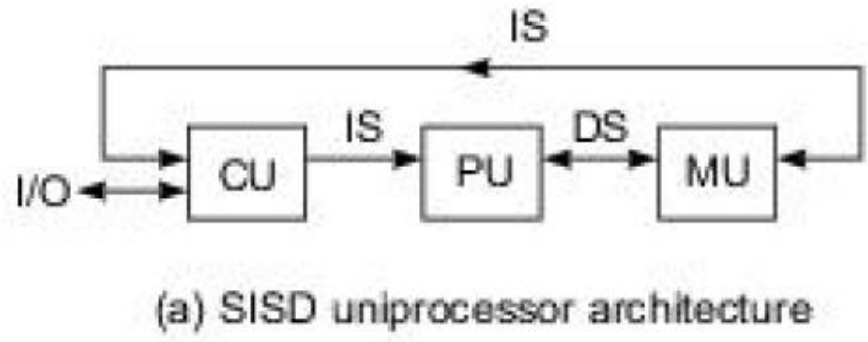
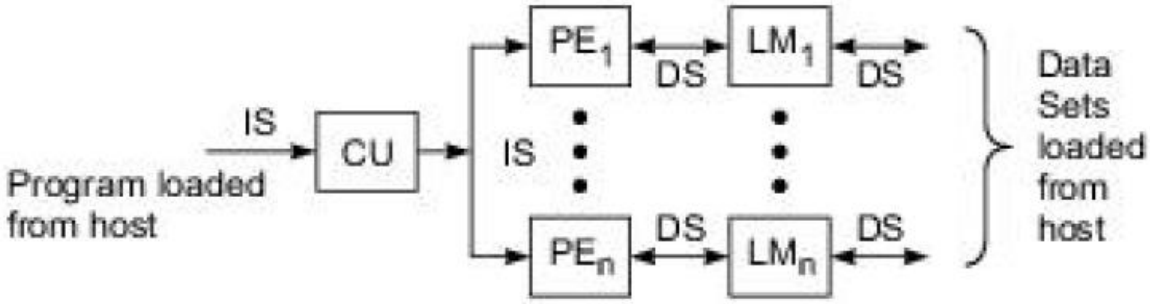


Fig. 1.2 Tree showing architectural evolution from sequential scalar computers to vector processors and parallel computers

2 **Explain Flynn's Classification of Computer architecture along with neat diagrams.**



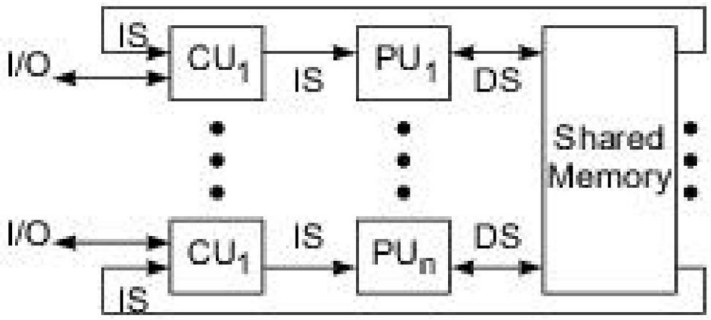
(a) SISD uniprocessor architecture



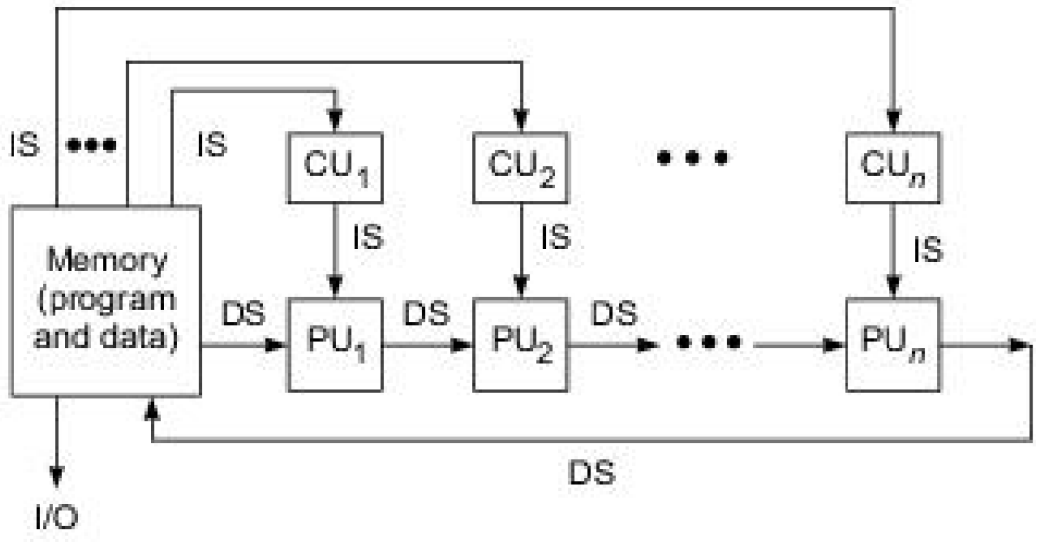
(b) SIMD architecture (with distributed memory)

Captions:

CU = Control Unit
PU = Processing Unit
MU = Memory Unit
IS = Instruction Stream
DS = Data Stream
PE = Processing Element
LM = Local Memory



(c) MIMD architecture (with shared memory)



(d) MISD architecture (the systolic array)

3 Explain UMA Model and COMA Model for shared memory multiprocessor systems, With neat diagram.

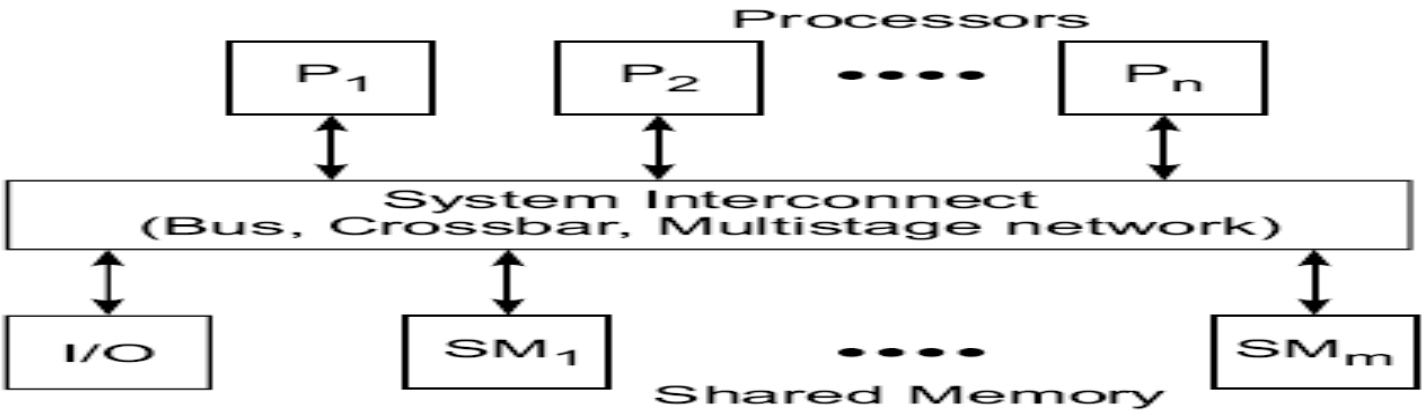
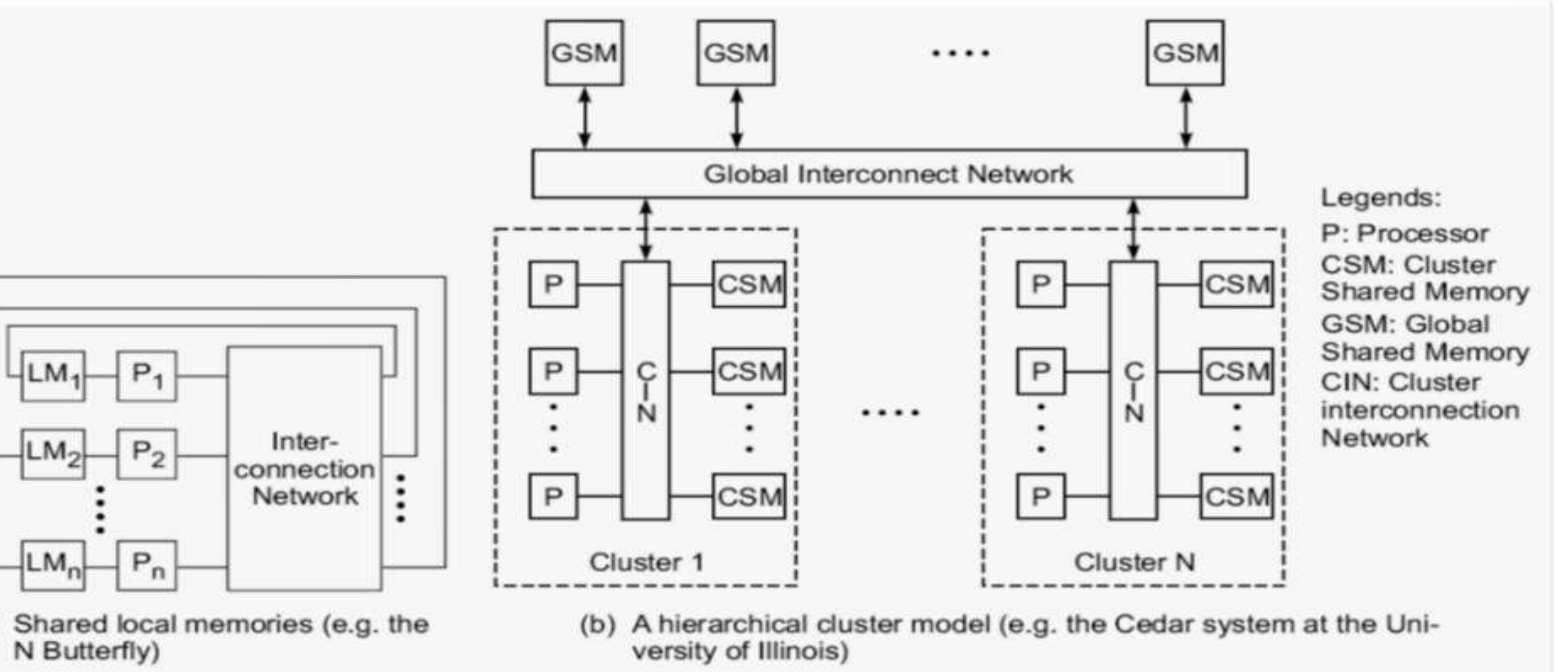


Fig. 1.6 The UMA multiprocessor model



Shared local memories (e.g. the N Butterfly)

(b) A hierarchical cluster model (e.g. the Cedar system at the University of Illinois)

Fig. 1.7 Two NUMA models for multiprocessor systems

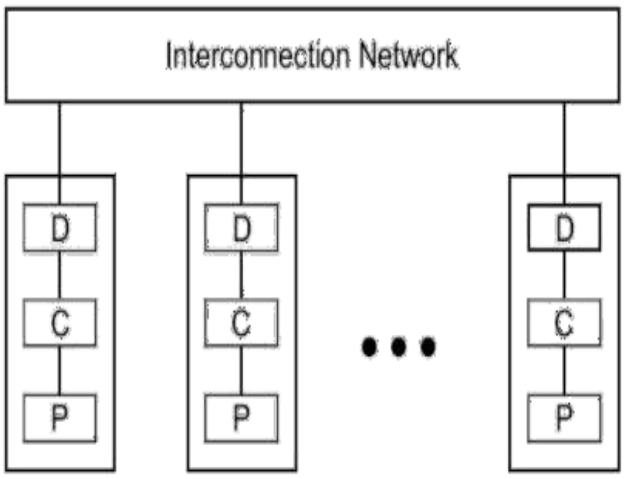


Fig. 1.8 The COMA model of a multiprocessor (P: Processor, C: Cache, D: Directory; e.g. the KSR-1)

4 Explain the Bernstein's conditions for parallelism. Detect parallelism in the following code using Bernstein's Conditions.

P1: C=D*E
P2:M=G+C
P3:A=B+C
P4:C=L+M
P5:G=G/E

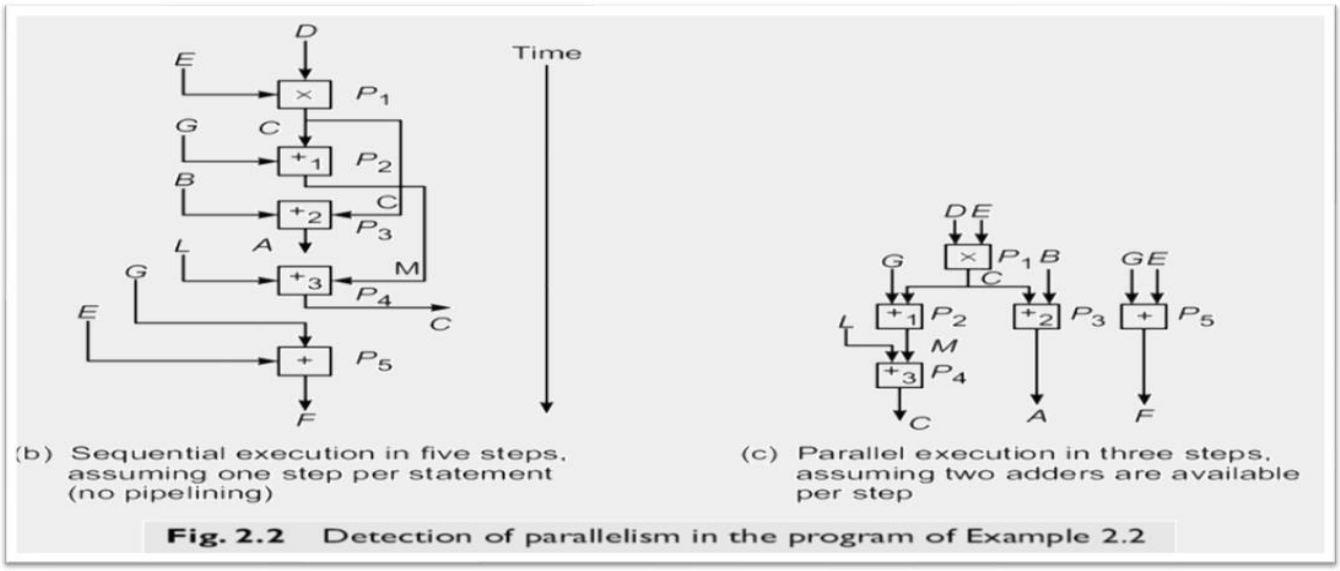


Fig. 2.2 Detection of parallelism in the program of Example 2.2

5. Find total processor clock cycles needed to execute a program. Consider the execution of an object code with 200000 instructions on a 20 MHZ processor. The program consists of four major types of instruction. The instruction mix and number of cycles (CPI) needed for each instruction is given below.

No	Instruction type	CPI	Instruction mix
1	Arithmetic and logic	1	68%
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i) Find total number of cycles required to execute the program.
ii) Calculate the CPI when the program is executed on uniprocessor system with above trace results.
iii) Calculate the MIPS rate based on CPI obtained in ii.

Solution

i.The formula for finding the total processor clock cycles is given below

$$\text{CPU clock cycles} = \sum_{i=1}^{n} IC_i \times CPI_i$$

CPU Clock cycles= [(68% *200000) *1] + [(8% * 200000)*2] + [(14*200000)*4] + [(10% * 200000)*8] = **440000**

ii. The formula for finding the total CPI is given below

CPI = Σ Frequency$_i$ * CPI$_i$

CPI = (0.68*1) + (0.08x2) + (0.14*4) + (0.1*8) = **2.2**

iii) The formula for finding the MIPS rate is given below

MIPS rate = clock rate / (CPI *10^6)

MIPS rate = (20*10^6) / (2.2* 10^6)
= 9.09

6. Explain the architecture of Vector super Computer with a neat diagram

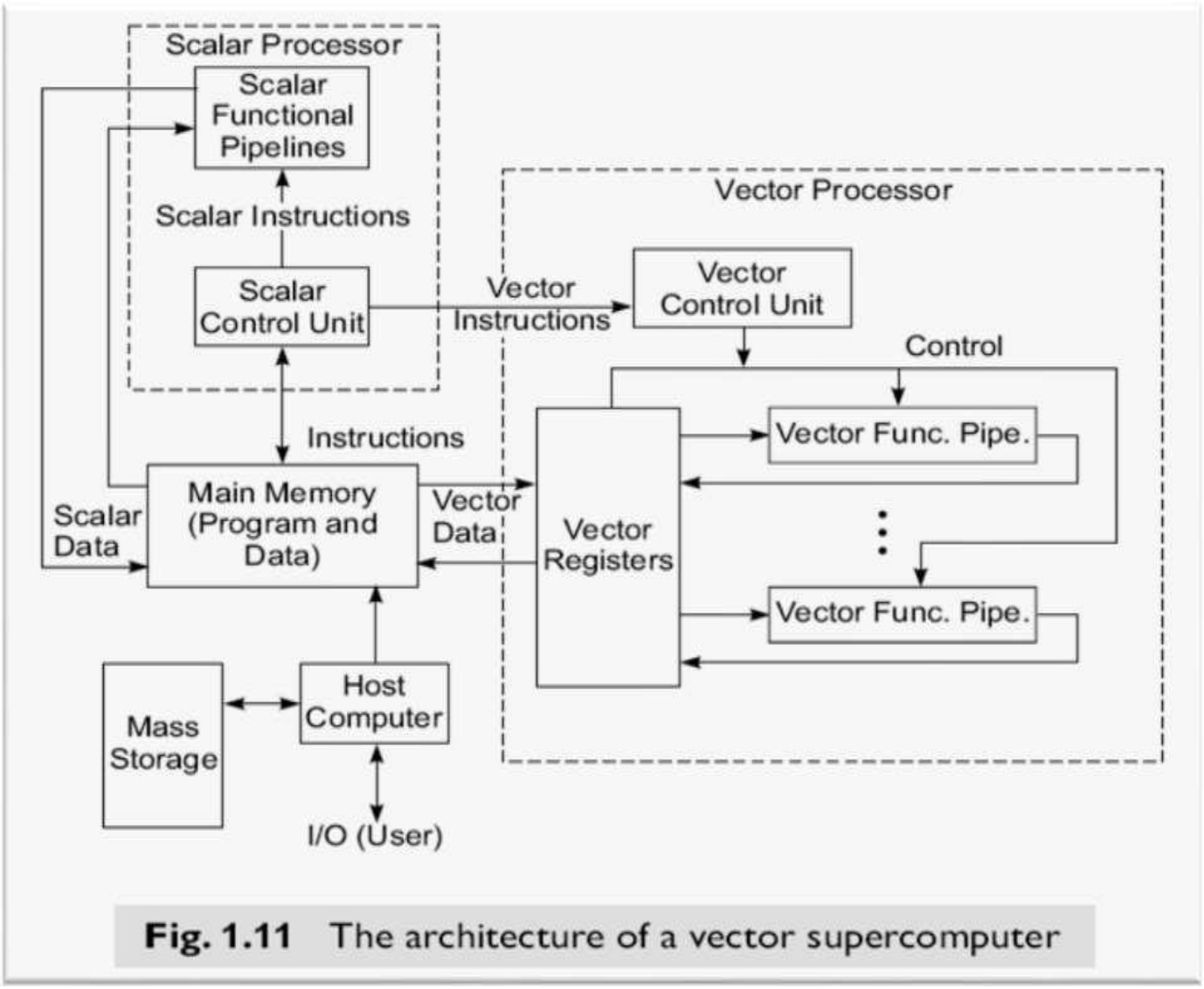

Fig. 1.11 The architecture of a vector supercomputer

7 (a) What are the factors affecting the scalability of computing systems, briefly explain.

(b) List the performance factors and system attributes that influence the performance of a computing system

- A sequential algorithm is evaluated in terms of its execution time which is expressed as a function of its input size.
- For a parallel algorithm, the execution time depends not only on input size but also on factors such as parallel architecture, no. of processors, etc

Performance Metrics

Parallel Run
Time Speedup
Efficiency

Standard Performance Measures

Peak Performance
Sustained Performance Instruction

Execution Rate (MIPS)
Floating point capability(MFLOPS)
Parallel Runtime

The parallel run time T(n) of a program or application is the time required to run the program on an n-processor parallel computer. When n = 1, T(1) denotes sequential runtime of the program on a sequential processor

Speedup

Speedup S(n) is defined as the ratio of time taken to run a program on a single processor to the time taken to run the program on a parallel computer with identical processors

Scalability of parallel Algorithms- Characteristics

- Deterministic vs non-deterministic
- Computational granularity
- Parallelism profile
- Communication patterns and Synchronization requirements
- Uniformity of the operations
- Memory requirement and data structures

8 With a neat diagram explain the operational model of SIMD super computer

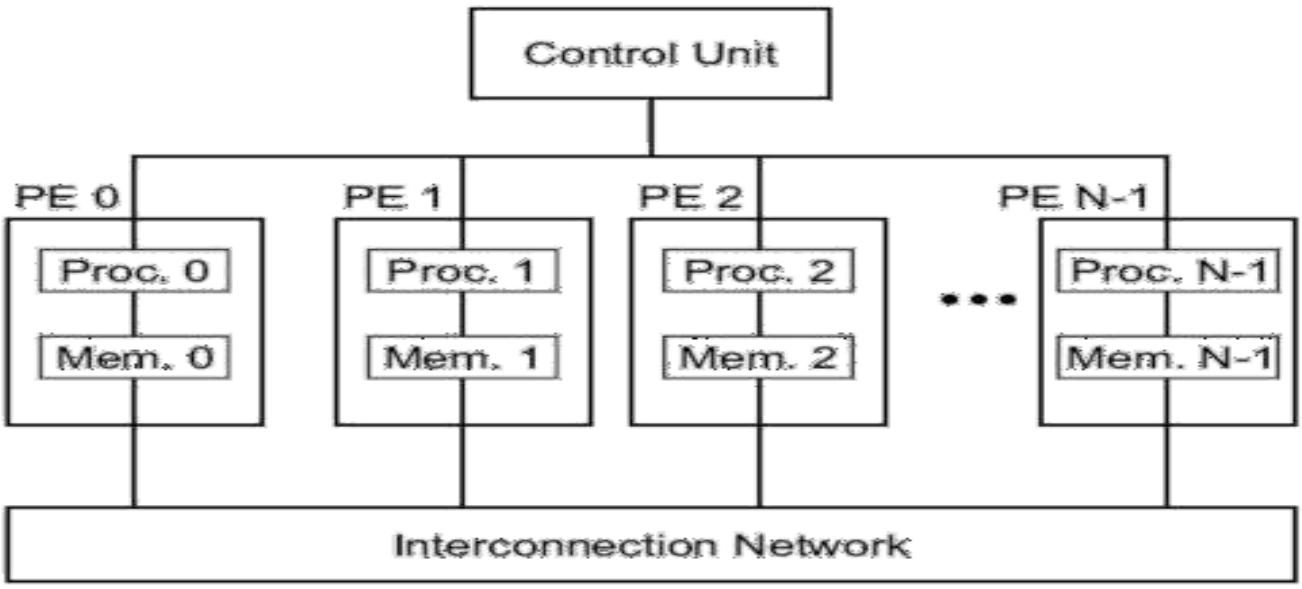

Fig. 1.12 Operational model of SIMD computers