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Internal Assessment Test 2 – January 2022

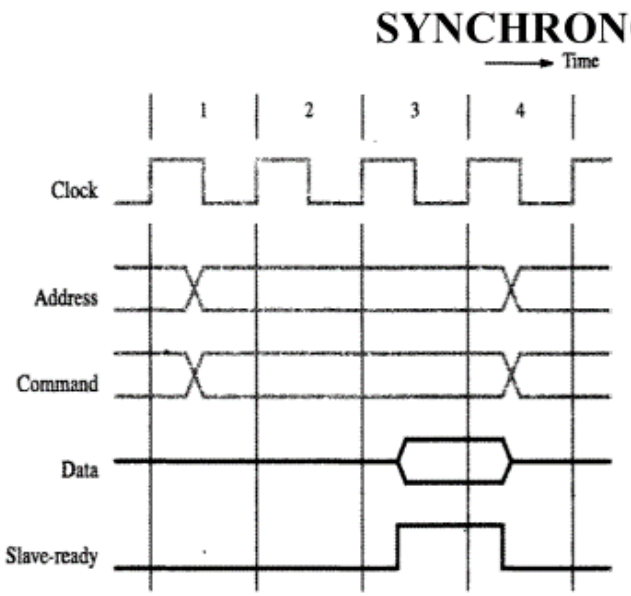
Sub:	Computer Organization					Sub Code:	18CS34	Branch:	CSE	
Date:	25/01/22	Duration:	90 minutes	Max Marks:	50	Sem / Sec:	III / A, B, C		OBE	
	Answer any FIVE FULL Questions							MARKS	CO	RBT
1	Elucidate the Synchronous and Asynchronous Bus in detail.							[10]	2	L1
2 (a)	With neat sketch, explain the general 8-bit parallel interface.							[6]	2	L1
(b)	Write short notes on SCSI bus signals.							[4]	2	L1
3 (a)	Explain the process of read operation on the PCI Bus along with clock diagram							[6]	2	L1
(b)	Illustrate the tree structure of USB with diagram							[4]	2	L1
4	Demonstrate how data are written onto a ROM cell. Discuss the different types of Read Only Memories.							[10]	3	L2
5	Explain in detail the 3 types of determining the cache locations to store the main memory blocks.							[10]	3	L2
6 (a)	What is memory interleaving. Explain.							[6]	3	L1
(b)	A block-set-associate cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. (i) How many bits are there in a main memory address? (ii) How many bits are there in each of the TAG, SET and WORD fields ?							[4]	3	L2

CMR INSTITUTE OF TECHNOLOGY, BANGALORE
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
INTERNAL ASSESSMENT – 2 (Scheme & Solution)

Semester: 3 Date: 25/01/2022
Subject: COMPUTER ORGANIZATION (18CS34)
Faculty: Prof. Savitha S, Dr. R. Kesavamoorthy Max Marks: 50

ANSWER_ANY 5 Question(s)

Question #		Description	Marks Distribution		Max Marks

1	a)	Elucidate the Synchronous and Asynchronous Bus in detail.
		
		Synchronous Bus – 5 Marks
		
		 
		
		Figure 4.25 An input transfer using multiple clock cycles.
		
		• Limitations
		  • Forces all the devices to operate at the speed of the slowest device
		  • What if the device doesn't respond
		• Control signal to respond
		• Clock Cycle 1
		  • Master sends address and command information
		• Clock Cycle 2
		  • Slave receives the info and decodes
		  • Prepares the data to send
		• Clock Cycle 3
		  • Slave places the data
		  • Slave sends Slave Ready signal
		  • Master strobes the data into its input buffer
		• Clock Signals
		  • Processor – 500 MHz typical
		  • I/O and Memory Bus – 150 MHz Maximum
			5	10	10

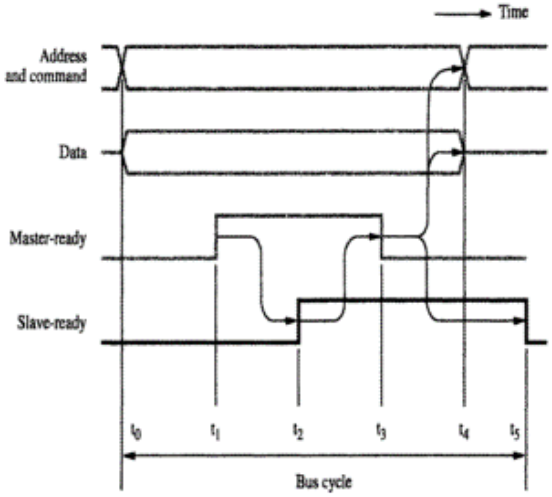
		Asynchronous Bus – 5 Marks **ASYNCHRONOUS BUS**  **Figure 4.27** Handshake control of data transfer during an output operation. • At t_0, • Master places Addr & Commd info • Master also places data • At t_1, • Master sends Master ready signal • At t_2, • Slave sends Slave ready signal • Slave strobes the data • At t_3, • Slave ready signal reaches Master • Master drops Master ready signal • At t_4, • Master removes Addr, Commnd, and data • At t_5, • Device interface will complete the transfer	5		
2	a)	With neat sketch, explain the general 8-bit parallel interface. **Explanation – 3 Marks** • Data-lines **P_7** through **P_0** can be used for either input or output purposes (Figure 4.34). • For increased flexibility, → some lines can be used as inputs and → some lines can be used as outputs. • The **DATAOUT** register is connected to data-lines via 3-state drivers that are controlled by a **DDR**. • The processor can write any 8-bit pattern into DDR. (DDR → Data Direction Register). • If DDR=1, Then, data-line acts as an output-line; Otherwise, data-line acts as an input-line. • Two lines, **C_1** and **C_2** are used to control the interaction between interface-circuit and I/0 device. Two lines, C_1 and C_2 are also programmable. • Line C_2 is bidirectional to provide different modes of signaling, including the handshake. • The **Ready** and **Accept** lines are the handshake control lines on the processor-bus side. Hence, the Ready and Accept lines can be connected to Master-ready and Slave-ready. • The input signal **My-address** should be connected to the output of an address-decoder. The address-decoder recognizes the address assigned to the interface. • There are 3 register select lines: **RS_0-RS_2**. Three register select lines allows up to eight registers in the interface. • An interrupt-request **INTR** is also provided. INTR should be connected to the interrupt-request line on the computer-bus.	3	6	10

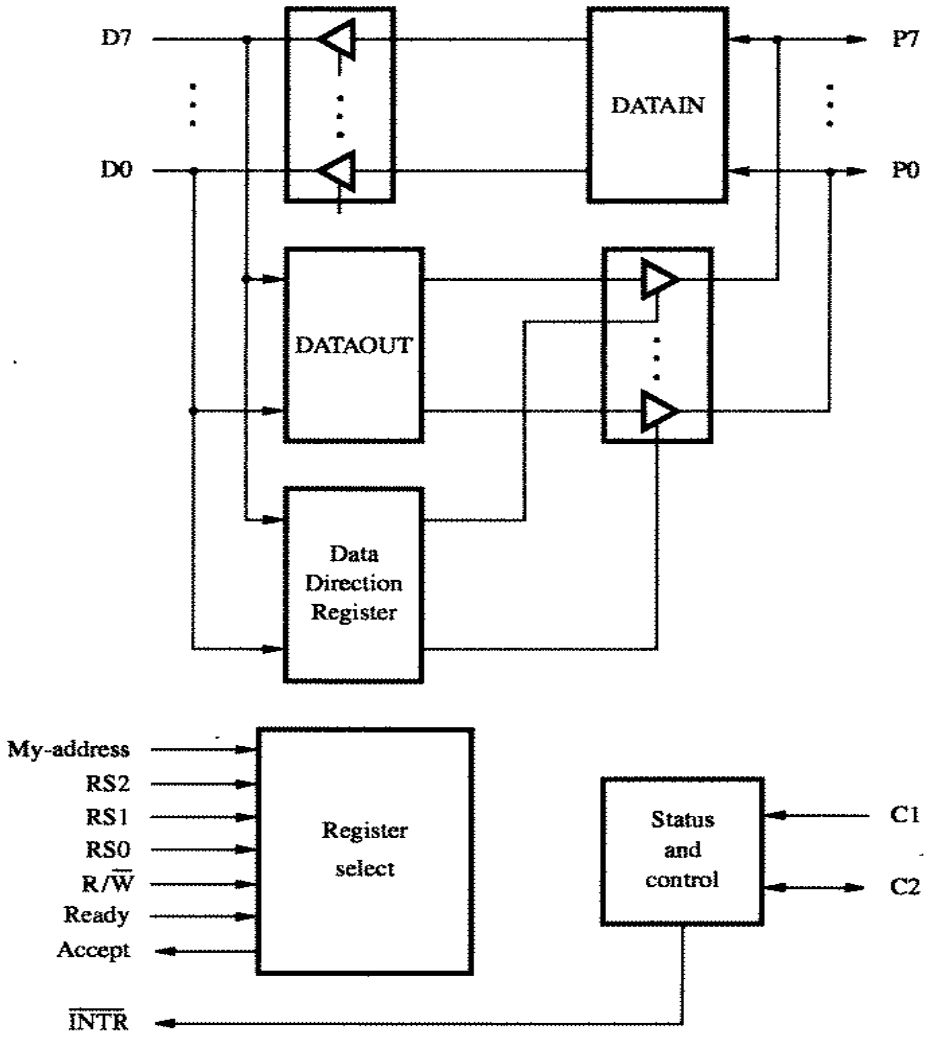
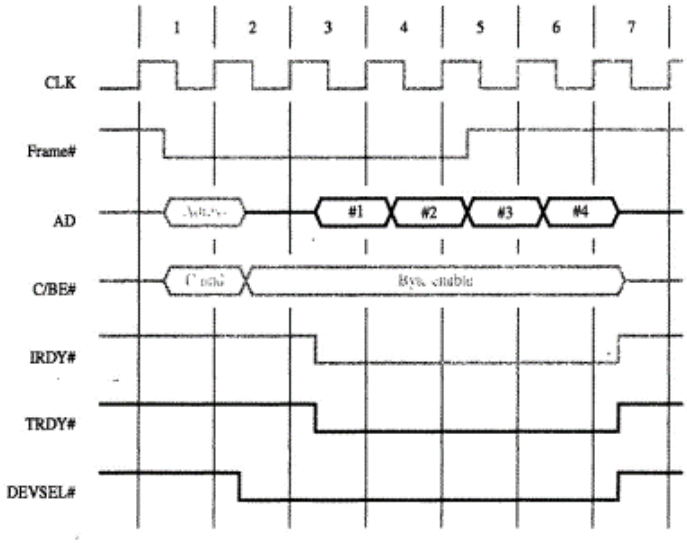
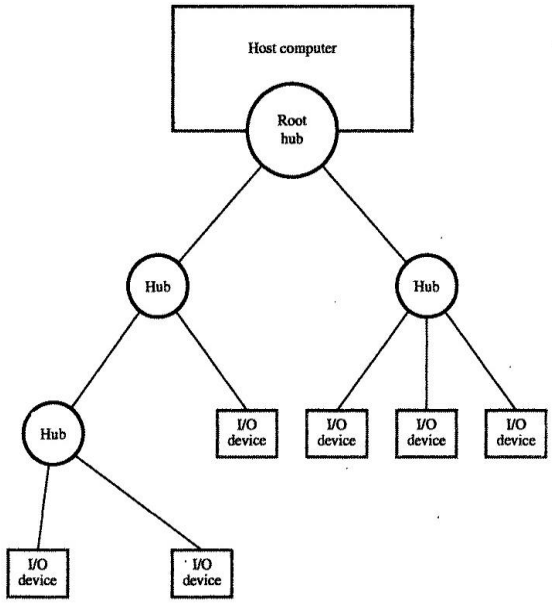
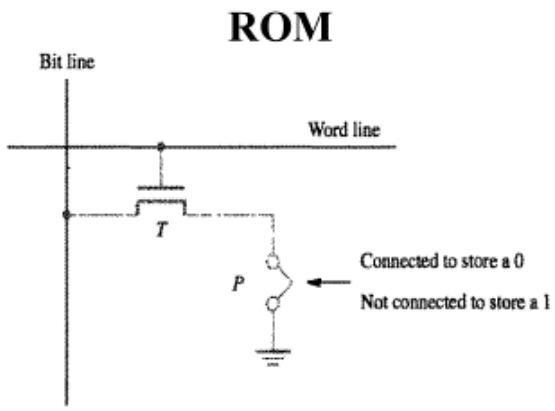
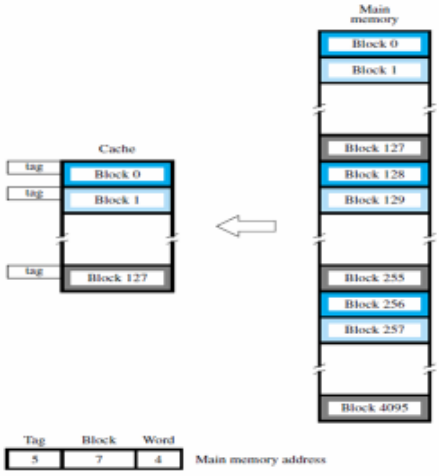
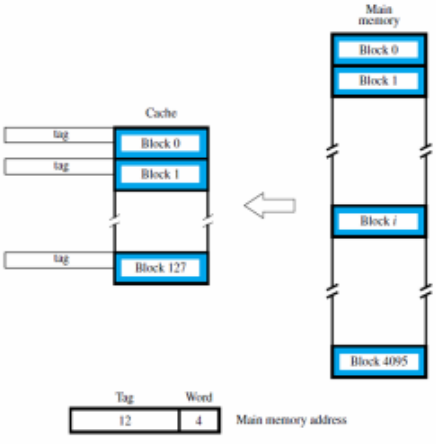
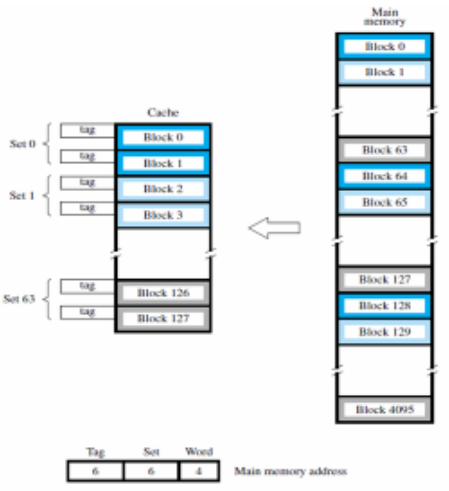
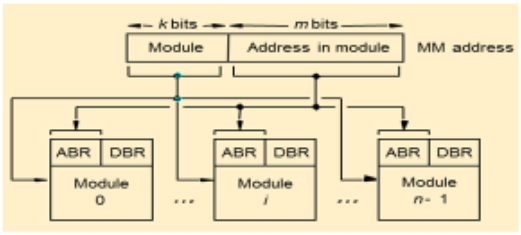
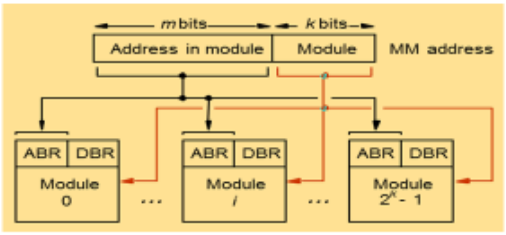
		Figure – 3 Marks  **Figure 4.34** A general 8-bit parallel interface.	3		
b)		Write short notes on SCSI bus signals. **Any 4 bus signal with Name, Category and Function – Each 1 Mark**		4	

		Table 4.4 The SCSI bus signals **Category** / **Name** / **Function** Data: –DB(0) to –DB(7) — Data lines: Carry one byte of information during the information transfer phase and identify device during arbitration, selection and reselection phases –DB(P) — Parity bit for the data bus Phase: –BSY — Busy: Asserted when the bus is not free –SEL — Selection: Asserted during selection and reselection Information type: –C/D — Control/Data: Asserted during transfer of control information (command, status or message) –MSG — Message: indicates that the information being transferred is a message Handshake: –REQ — Request: Asserted by a target to request a data transfer cycle –ACK — Acknowledge: Asserted by the initiator when it has completed a data transfer operation Direction of transfer: –I/O — Input/Output: Asserted to indicate an input operation (relative to the initiator) Other: –ATN — Attention: Asserted by an initiator when it wishes to send a message to a target –RST — Reset: Causes all device controls to disconnect from the bus and assume their start-up state	4		
3	a)	Explain the process of read operation on the PCI Bus along with clock diagram **Figure – 3 Marks** **PCI – DATA TRANSFER**  **Figure 4.40** A read operation on the PCI bus.	3	6	10

		Explanation – 3 Marks **PCI – DATA TRANSFER** • During Clock cycle-1, ➢ The processor a → asserts FRAME# to indicate the beginning of a transaction; → sends the address on AD lines and command on C/BE# Lines. • During Clock cycle-2, ➢ The processor removes the address and disconnects its drives from AD lines. ➢ Selected target → enables its drivers on AD lines and → fetches the requested-data to be placed on bus. ➢ Selected target → asserts DEVSEL# and → maintains it in asserted state until the end of the transaction. ➢ C/BE# is → used to send a bus command and it is → used for different purpose during the rest of the transaction. • During Clock cycle-3, ➢ The initiator asserts IRDY# to indicate that it is ready to receive data. ➢ If the target has data ready to send then it asserts TRDY#. In our eg, the target sends 3 more words of data in clock cycle 4 to 6. • During Clock cycle-5 ➢ The indicator uses FRAME# to indicate the duration of the burst, since it read 4 words, the initiator negates FRAME# during clock cycle 5. • During Clock cycle-7, ➢ After sending 4th word, the target → disconnects its drivers and → negates DEVSEL# during clock cycle 7.	3		
	b)	Illustrate the tree structure of USB with diagram **Figure – 2 Marks**  **Figure 4.43** Universal Serial Bus tree structure.	2	4	

		Explanation – 2 Marks **USB ARCHITECTURE** • To accommodate a large number of devices that can be added or removed at any time, the USB has the tree structure as shown in the figure 7.17. • Each node of the tree has a device called a **Hub.** • A hub acts as an intermediate control point between the host and the I/O devices. • At the root of the tree, a **Root Hub** connects the entire tree to the host computer. • The leaves of the tree are the I/O devices being served (for example, keyboard or speaker). • A hub copies a message that it receives from its upstream connection to all its downstream ports. • As a result, a message sent by the host computer is broadcast to all I/O devices, but only the addressed-device will respond to that message.	2		
4		Demonstrate how data are written onto a ROM cell. Discuss the different types of Read Only Memories. **ROM Cell – 2 Marks**  **Figure 5.12** A ROM cell. ➢ **At Logic value '0'** → Transistor(T) is connected to the ground point (P). Transistor switch is closed & voltage on bit-line nearly drops to zero ➢ **At Logic value '1'** → Transistor switch is open. The bit-line remains at high voltage. **Different Types of ROM – 8 Marks (4 Types – Each 2 Marks)** • PROM (Programmable Read Only Memory) • EPROM (Erasable Programmable Read Only Memory) • EEPROM (Electrically Erasable Programmable Read Only Memory) • Flash	2 8	10	10

5		Explain in detail the 3 types of determining the cache locations to store the main memory blocks. **Three mapping functions:** • Direct mapping (3 Marks) • Associative mapping (3.5 Marks) • Set-Associative mapping. (3.5 Marks) Direct Mapping  •*Block j of the main memory maps to **j modulo 128** of the cache. 0 maps to 0, 129 maps to 1.* •*More than one memory block is mapped onto the same position in the cache.* •*May lead to contention for cache blocks even if the cache is not full.* •*Resolve the contention by allowing new block to replace the old block, leading to a trivial replacement algorithm.* •*Memory address is divided into three fields:* *- **Low order 4** bits determine one of the 16 words in a block.* *- When a new block is brought into the cache, the **next 7 bits** determine which cache block this new block is placed in.* *- **High order 5 bits** determine which of the possible 32 blocks is currently present in the cache.* *These are tag bits.* •*Simple to implement but not very flexible.* Associative mapping  •*Main memory block can be placed into any cache position.* •*Memory address is divided into two fields:* *- Low order 4 bits identify the word within a block.* *- High order 12 bits or tag bits identify a memory block when it is resident in the cache.* •*Flexible, and uses cache space efficiently.* •*Replacement algorithms can be used to replace an existing block in the cache only when the cache is full.* •*Cost is higher than direct-mapped cache because of the need to search (Associative Search) all 128 patterns to determine whether a given block is in the cache.* •*The tag bits of an address received from the processor are compared to the tag bits of each block of the cache.* **Advantage of associative mapping:** 1. There is flexibility when mapping a block to any block of the cache **Disadvantages of associative mapping:** 1. A replacement algorithm must be used to determine which block of cache to swap out 2. More space is needed for the tag field 3. The most important disadvantage is the complex circuitry needed to examine all of the tags in parallel in the cache	3 3.5	10	10

		Set-Associative Mapping  •*Blocks of cache are grouped into sets.* •*Mapping function allows a block of the main memory to reside in any block of a specific set.* •*Divide the cache into 64 sets, with two blocks per set.* •*Memory block 0, 64, 128 etc. map to block 0, and they can occupy either of the two positions.* •*Memory address is divided into three fields:* *- 6 bit set field determines the set number. (64 sets)* *- High order 6 bit fields are compared to the tag fields of the two blocks in a set.* •*Set-associative mapping is combination of direct and associative mapping.* •*Contention problem is eased by having few choices for placement.* •*Size of the associative search is decreased.*	3.5		
6	a)	What is memory interleaving. Explain. **Figure – 3 Marks** **Methods of Address Layouts**  ▪ ***Consecutive words are placed in a module.*** ▪ ***High-order k bits*** *of a memory address determine the module.* ▪ ***Low-order m bits*** *of a memory address determine the word within a module.* ▪ *When a block of words is transferred from main memory to cache, only one module is busy at a time.*  •***Consecutive words are located in consecutive modules.*** •***Low-order k bits*** *select a module* •***High-order m bits*** *determine the word within module* •*Consecutive addresses can be located in consecutive modules.* •*While transferring a block of data, several memory modules can be kept busy at the same time.* **Explanation – 3 Marks**	3 3	6	10
	b)	A block-set-associate cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. (i) How many bits are there in a main memory address? (ii) How many bits are there in each of the TAG, SET and WORD fields ?			

		Main Memory size=4096 blocks x128 words =4x1024x128 =22x210x27=219 Hence number of bits for address is 19-bits Word – 7 Set – 4 Tag – 8 bit	1 1 1 1	4	