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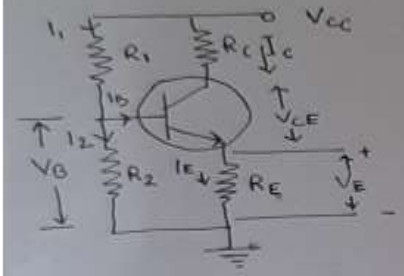
Sub:	Analog and Digital Electronics					Sub Code:	18CS33
Date:	07/03/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	3rd / A,B,C

Answer any FIVE FULL Questions

1 (a) **Explain voltage divider bias circuit with the neat circuit diagram and necessary derivations**

Ans:

Voltage Divider bias by approximate analysis



This biasing is also known as emitter-current bias and also provides the most stable operating point (I_C, V_{CE}) compared to other bias.

In this circuit, the levels of I_C & V_{CE} are independent of h_{fe} or β value.

In this CKt, R_1 & R_2 constitutes a voltage divider that divides the supply voltage V_{cc} to produce base voltage V_B.

Applying KCL, we have,

$$I_1 = I_2 + I_B$$

This ckt is designed in such a way, so that, voltage divider current $I_2 >>$ Base current I_B,

hence, $I_2 >> I_B$, therefore $I_1 \approx I_2$

By applying KVL in the inner loop,

$$V_{cc} = I_1 R_1 + I_2 R_2$$

as, $I_1 \approx I_2$, then, $V_{cc} = I_1 R_1 + I_1 R_2 = I_2 R_1 + I_2 R_2$

$$\therefore I_2 = \frac{V_{cc}}{R_1 + R_2}$$

Voltage accross R_2 is V_B

$$\therefore I_2 R_2 = V_B \Rightarrow V_B = \frac{V_{cc}}{R_1 + R_2} R_2$$

Voltage accross R_E is V_E,

$$\therefore V_E = I_E R_E$$

Applying KVL to Base - Emitter loop,

$$V_B - V_{BE} - V_E = 0$$

$$\therefore V_E = V_B - V_{BE}$$

$$\therefore I_E R_E = V_B - V_{BE}$$

$$\therefore I_E = \frac{V_B - V_{BE}}{R_E} \approx I_C$$

Now, applying KVL to outer loop,

$$V_{cc} = I_C R_C + V_{CE} + I_E R_E$$

$I_C \approx I_E$

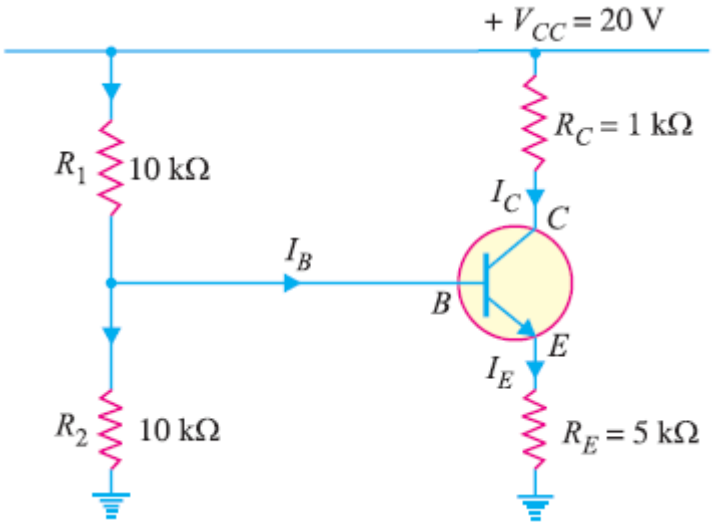
$$\therefore V_{cc} = I_C R_C + V_{CE} + I_C R_E$$

$$\therefore V_{CE} = V_{cc} - I_C (R_C + R_E)$$

$$\therefore V_{CE} = V_{cc} - \frac{(V_B - V_{BE})(R_C + R_E)}{R_E}$$

$$\therefore V_{CE} = V_{cc} - (V_B - V_{BE})\left(1 + \frac{R_C}{R_E}\right)$$

(b) **Calculate the emitter current in the voltage divider circuit shown in Fig.below. Also find the value of V_{CE} and collector potential V_C. Amplification factor = 100.**



ANS:

d.c. load line :

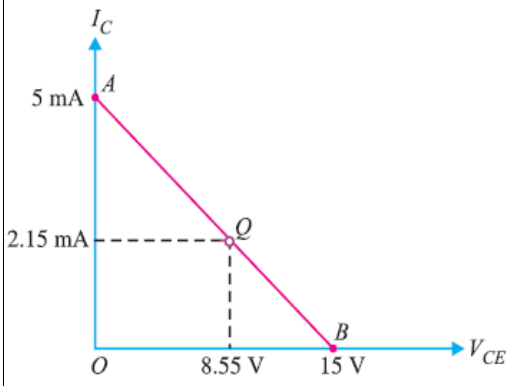
The collector-emitter voltage V_{CE} is given by

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15\text{V}$. This locates the first point B ($OB = 15\text{V}$) of the load line on the collector-emitter voltage axis.

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15\text{ V}}{(1+2)\text{ k}\Omega} = 5\text{ mA}$$

This locates the second point A (OA = 5 mA) of the load line on the collector current axis. By joining points A and B, the d.c. load line AB is constructed as shown in Fig.



For silicon transistor, V_{BE} = 0.7 V

Voltage across 5 kΩ is

$$V_2 = \frac{V_{CC}}{10+5} \times 5 = \frac{15 \times 5}{10+5} = 5 \text{ V}$$

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \text{ k}\Omega} = \frac{4.3 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

$\therefore$ Collector current is

$$I_C \simeq I_E = 2.15 \text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 15 - 2.15 \text{ mA} \times 3 \text{ k}\Omega = 15 - 6.45 = 8.55 \text{ V}$$

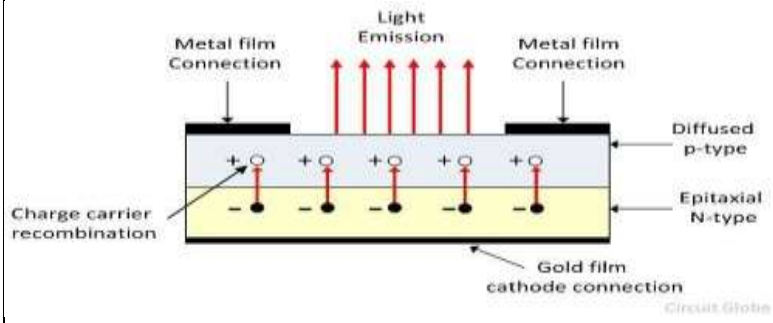
$\therefore$ Operating point is **8.55 V, 2.15 mA.**

Fig. above shows the operating point Q on the load line. Its co-ordinates are I_C = 2.15 mA, V_{CE} = 8.55 V

2 **Explain the construction, working principles and applications of light-emitting diode (LED). ANS:.**

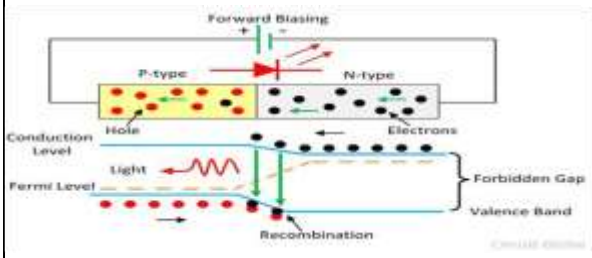
LED : Construction

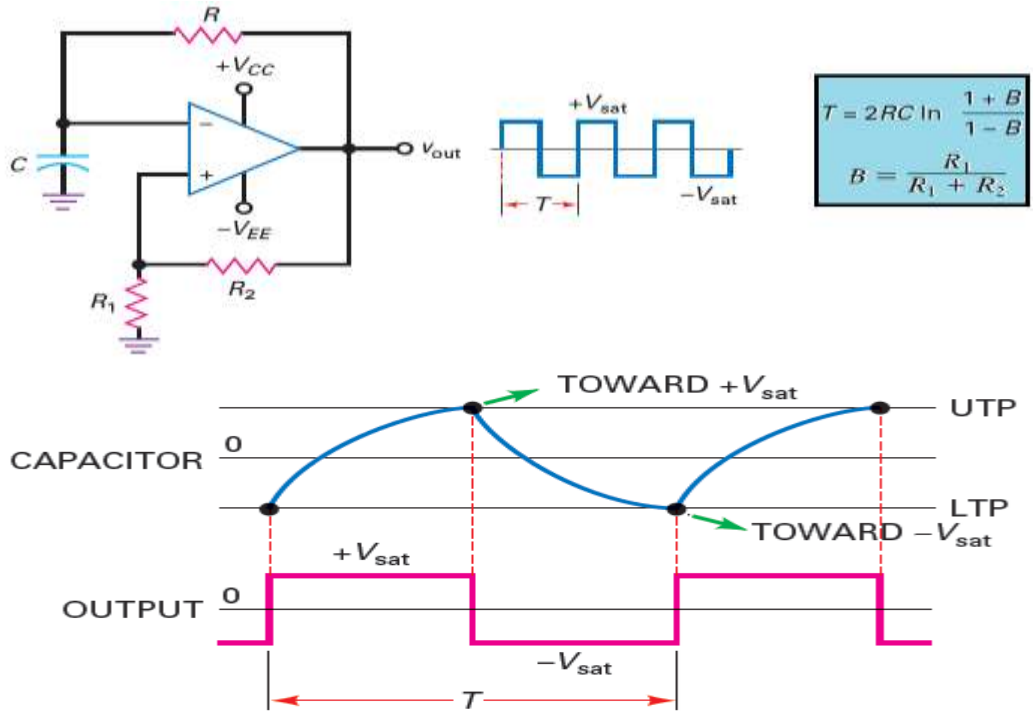
- The semiconductor material used in LED is Galliurn Arsenide (GaAs), Gallium phosphide (GaP) or Gallium Arsenide Phosphide (GaAsP).
- The semiconductor layer of P-type is placed above N-type because the charge carrier recombination occurs in P-type.
- If *P-type is placed below the N-type, the emitted light cannot be seen.*



LED : Working Principle

1. The charge carriers recombine in a forward-biased P-N junction as the electrons cross from the N-region and recombine with the holes existing in the P-region.
2. Free electrons are in the conduction band of energy levels
3. Holes are in the valence energy band.
4. Energy level of the holes is less than the energy levels of the electrons.
5. Some portion of the energy must be dissipated to recombine the electrons and the holes. This energy is emitted in the form of heat and light.
6. Electron emit electromagnetic energy in the form of photons.
7. The energy of photons is equal to the gap between the valence and the conduction band.
8. Color of light can be determined by the band gap of semiconductor material



	LEDs Applications Used in music system for digital display Used in traffic signals for controlling the traffic crowds in cites. Used in digital computers for displaying the computer data Used in microwave to display timing Used in railway signals Used in segment display in digital kits Remote control systems such TV or LCD remote. Used in electronic calculators for showing the digital data. Used in digital watches and automotive heat lamps.
3	**Explain the construction and working of the Relaxation oscillator.** **ANS:**  A **relaxation oscillator** is the one which satisfies all the below conditions: • It must provide a non-sinusoidal waveform (of either voltage or current parameter) at the output. • 2.It must provide a periodic signal or repetitive signal like Triangular, Square or Rectangular wave at the output. • The circuit of a relaxation oscillator must be a nonlinear one. That means the design of the circuit must involve semiconductor devices like Transistor, MOSFET or OP-AMP. • The circuit design must also involve an energy storing device like a Capacitor or Inductor which charges and discharges continuously to produce a cycle. • The frequency or period of oscillation for such an oscillator depends on the time constant of their respective capacitive or inductive circuit. **Working principle :** • Initially, if we consider the output of the comparator is high, ○ then during this time the capacitor will be charging. ○ With the charging of the capacitor, its terminal voltage will gradually rise, which can be seen in the graph. • Once the capacitor terminal voltage reaches the threshold, the comparator output will go from high to low as shown in the graph. • And when the comparator output goes negative, the capacitor starts discharging to zero. • After the capacitor completely discharges because of the presence of a negative output voltage, it again charges except in the opposite direction.

- As you can see in the graph because of the negative output voltage, the capacitor voltage also rises in a negative direction.
- Once the capacitor charges to the maximum in a negative direction, the comparator switches output from negative to positive.
- Once the output switches to a positive cycle, the capacitor discharges in the negative path and builds up charges in the positive path as shown in the graph.
- So the cycle of capacitor charge and discharge in positive and negative paths trigger the comparator produces a square wave signal at the output which is shown above.

frequency of oscillation depends on the time constant of C and R in the circuit.

- Higher values of C and R will lead to longer charge and discharge rates, thus producing lower frequency oscillations.
- Similarly, smaller values will produce higher frequency oscillations.

Here R1 and R2 also play a critical role in determining the frequency of the output waveform.

- This is because they control the voltage thresholds that the C needs to charge up to

So the **Relaxation Oscillator Frequency Formula** will be:

$f = 1 / 2 \times R \times C \times \ln (1 + k / 1 - k)$

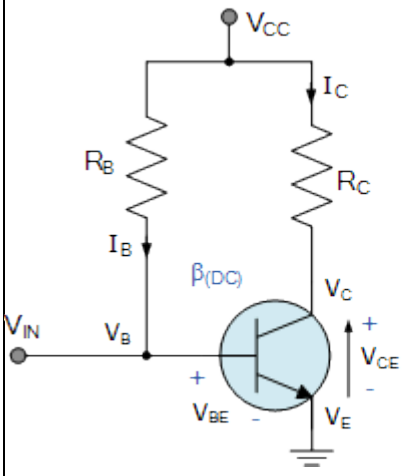
Here, $K = R_2 / R_1 + R_2$

If the resistors R1 and R2 are equal to each other, then

$f = 1 / 2.2 \times R \times C$

4 (a) **Explain base bias of BJT.**

(b) **ANS:**



$V_C = V_{CC} - (I_C R_C)$
$V_{CE} = V_C - V_E$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_{CC} - V_{BE}}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

The emitter diode of the transistor is forward biased by applying the required positive base bias voltage via the current limiting resistor R_B. Assuming a standard bipolar transistor, the forward base-emitter voltage drop would be 0.7V. Then the value of R_B is simply: $(V_{CC} – V_{BE})/I_B$ where I_B is defined as I_C/β.

With this single resistor type of biasing arrangement the biasing voltages and currents do not remain stable during transistor operation and can vary enormously. Also the operating temperature of the transistor can adversely effect the operating point.

Applying Kirchoff's Voltage Law (KVL) to the base circuit:

$V_{CC} - I_B R_B - V_{BE} = 0$

Or, $I_B = (V_{CC} - V_{BE})/R_B$ ---------- (1)

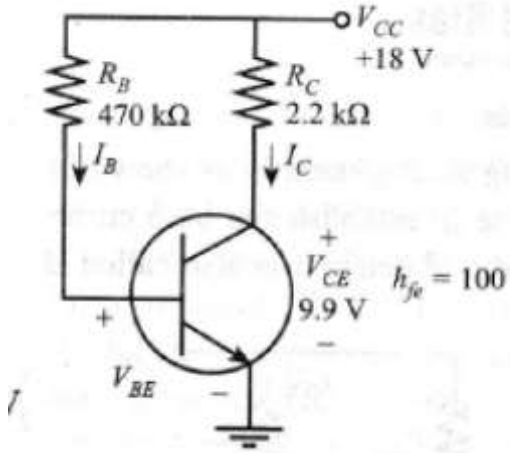
V_{BE} is 0.7 V for Silicon and 0.3 V for Germanium transistor.

Applying the KVL to the collector circuit:

$V_{CC} - I_C R_C - V_{CE} = 0$

Or, $V_{CE} = V_{CC} - I_C R_C$ ---------- (2)

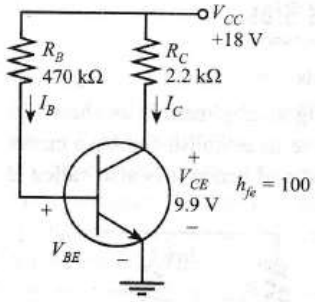
Calculate the values of IB,IC & VCE for the circuit shown in fig if RC=2.2KΩ, RB=470KΩ, VCC=18V, hfe=100. Draw the DC load line and Q point.



ANS:

Example 1:

The base bias circuit is shown in Figure for the values indicated calculate I_B, I_C and V_{CE}.



Given: $R_B = 470\ \text{k}\Omega$, $R_C = 2.2\ \text{k}\Omega$, $V_{CC} = 18\ \text{V}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 36.8\ \mu\text{A}$$

$$I_C = h_{fe} I_B = 100 \times 36.8\ \mu\text{A} = 3.68\ \text{mA}$$

$$V_{CE} = V_{CE} - I_C R_C = 18\ \text{V} - (3.68\ \text{mA} \times 2.2\ \text{k}\Omega) = 9.9\ \text{V}$$

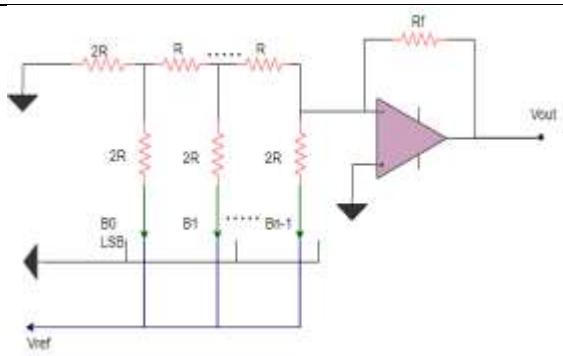
5 **Explain the working of R2R DAC with necessary circuit diagram & derivations.**

ANS:

R-2R configuration is a simple arrangement that consists of parallel and series resistors connected in the cascaded form to an operational amplifier

The following diagram shows the R-2R 3-bit ladder DAC.

- The leftmost side of the circuitry has the least significant bit i.e B0 whereas B2 which is the most significant bit is connected to the right side of the circuit to the amplifier.
- The binary inputs are given through the binary switches. So, when we need a high bit, the concerned bit is connected to the reference voltage and when a low bit is needed, the switch gets connected to the ground potential.

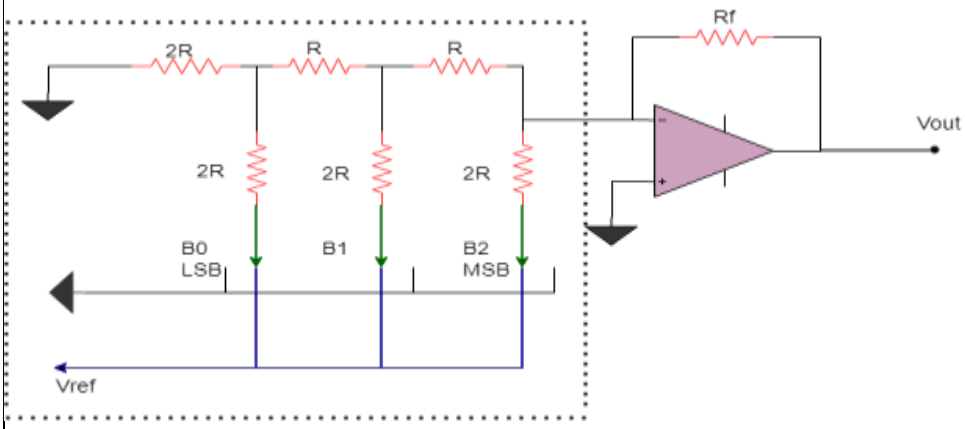


- The ladder arrangement consists of two resistors i.e. a base resistor R and a 2R resistor which is twice the value of the base resistor.
- This feature helps to maintain a precise output analog signal without using a wide range of resistor values.

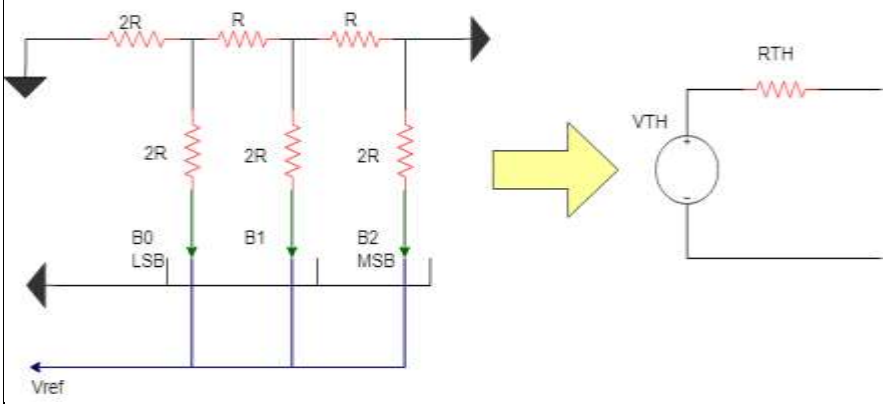
A pair of R and 2R is used for one input bit. The digital inputs are provided through binary switches connected to Vref for input as 1 and GND for input 0.

R-2R Ladder DAC Analysis with Thevenin Theorem

Thevenin's theorem is a technique through which we can obtain an equivalent circuit of the concerned resistance network. A Thevenin circuit consists of a Thevenin resistance and a Thevenin voltage that can be replaced in the circuit and work the same as the original resistance network.



RTh is calculated by short-circuiting all the voltage sources and replacing the current sources with open circuits.



When LSB is high

Let us first consider the binary code 001. Its VTh and RTh will be calculated in three stages.

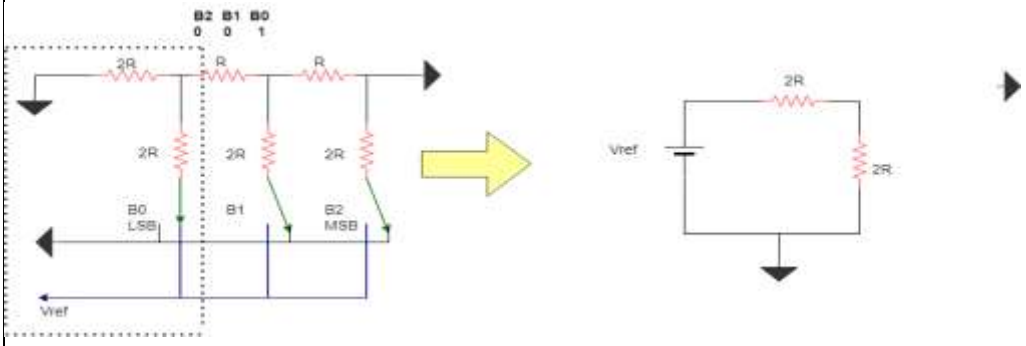
VTh= 2R x Vref / 2R+2R

VTh=Vref / 2

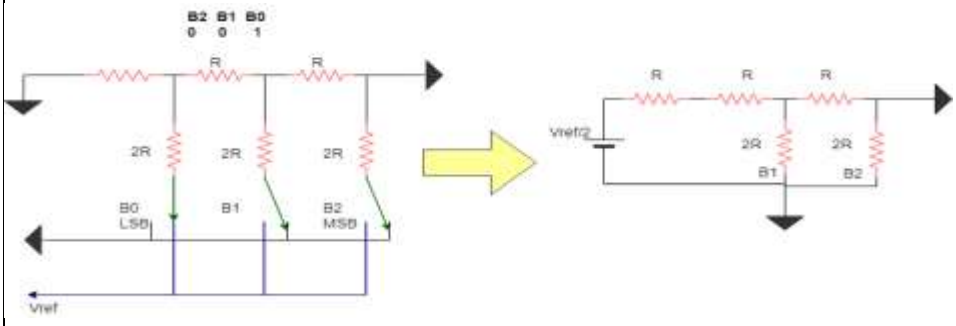
For measuring the Thevenin resistance, short circuit the reference voltage. Two resistances 2R and 2R become parallel to each other. So,

RTh=2R || 2R

RTh=R



Below is the equivalent circuit of the original after simplifying the first stage. The Thevenin equivalent of the first stage is connected in series to the rest of the circuit.



Now, we calculate the Thevenin circuit of the second stage. The dotted block will be solved in the second stage. Two resistors of the same value i.e R are connected in series. So it is replaced by equivalent resistance 2R shown in the given diagram below
The circuit is again configured to be a voltage divider with reference voltage as Vref/2. So,

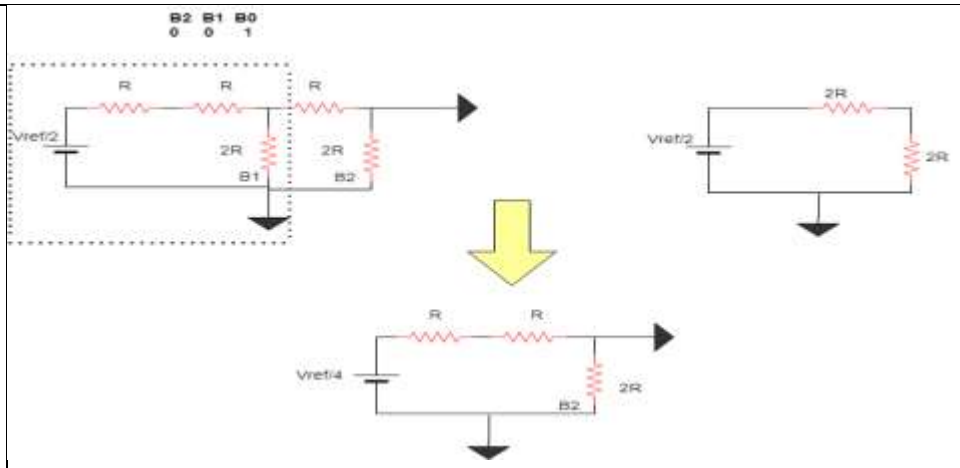
VTh= (2R x Vref/2) / 2R+2R

VTh=Vref / 4

for the Thevenin resistance, we consider the voltage source of this block to be zero. It gives the same Thevenin as the previous because of the exact arrangement and we will replace the concerned portion with equivalent Thevenin values

RTh=2R || 2R

RTh=R



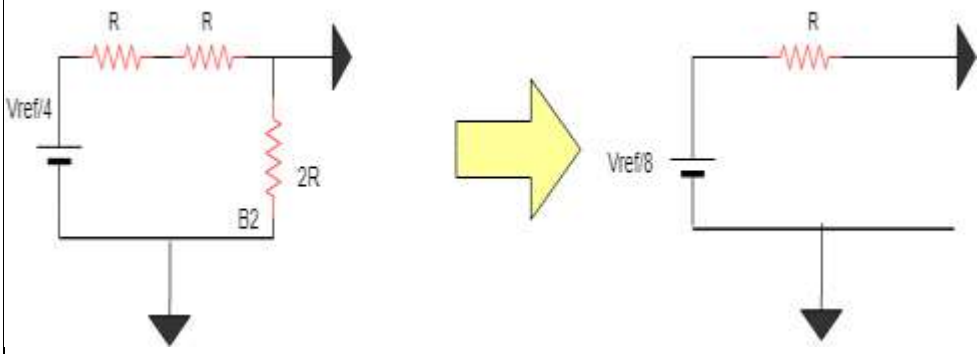
This is the resultant circuit which will be solved in the third stage. The VTh and RTh is as follows:

VTh= (2R x Vref/4) / 2R+2R

VTh=Vref / 8

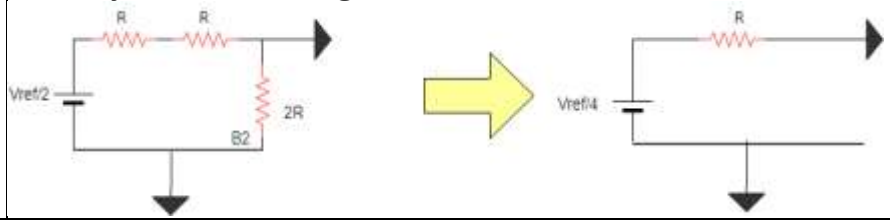
RTh=(R+R) || 2R

RTh=R

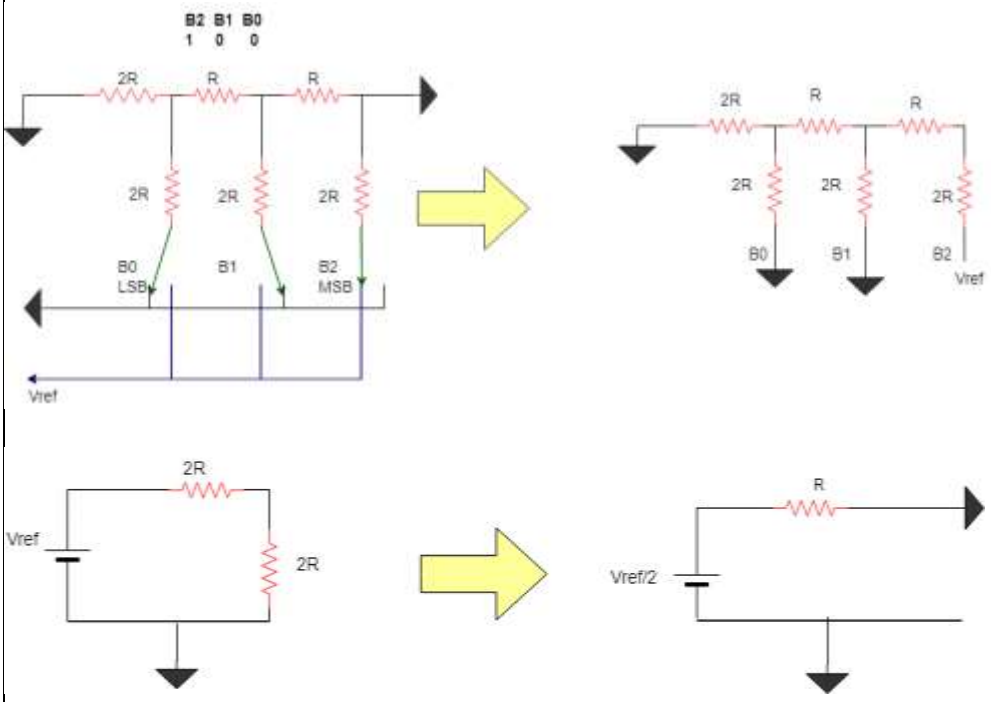


The solution depicts that whenever only B0 is connected to the reference voltage and B2=B1=0, the output voltage of the DAC would be Vref/8.

Similarly when the B1 high



When MSB Bit is high



When all three bits are high

When all 3 bits are connected to the reference voltage, the output voltage will be the superposition of all three voltages.

$Vr\text{-}2r = (Vref / 2)+(Vref / 4)+(Vref / 8)$

$Vr\text{-}2r = 7Vref / 8$

$Vr\text{-}2r = Vref\{B0/2^{(N)} + B0/2^{(N-1)} + B0/2^{(N-2)} + \ldots + B0/2^2 + B0/2^1 \}$

Where N is the number of bits.

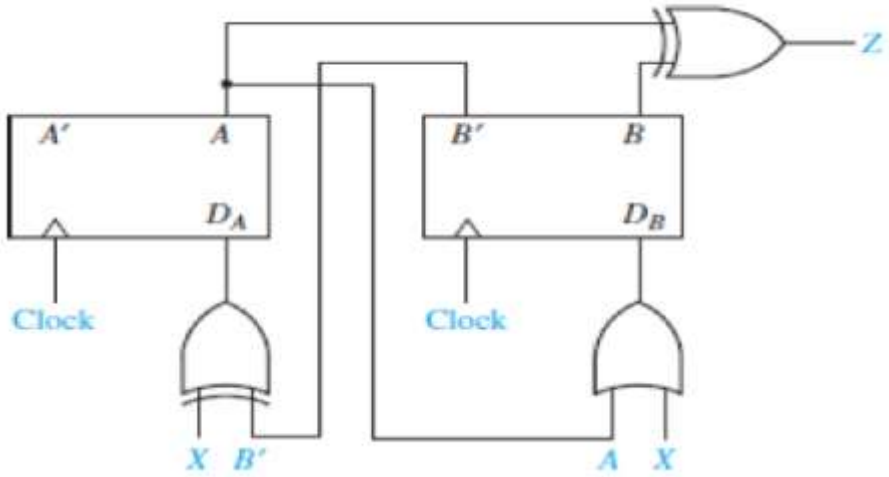
Vr-2r is applied to the inverting operational amplifier and the output voltage is measured. The output would be 180 degrees out of phase with the input Vr-2r. The following is the general output voltage equation of R-2R DAC

$Vout = -(Rf/R) \times Vr\text{-}2r$

$Vout = -(Rf/R)\{B0/2^{(N)} + B0/2^{(N-1)} + B0/2^{(N-2)} + \ldots + B0/2^2 + B0/2^1 \}Vref$

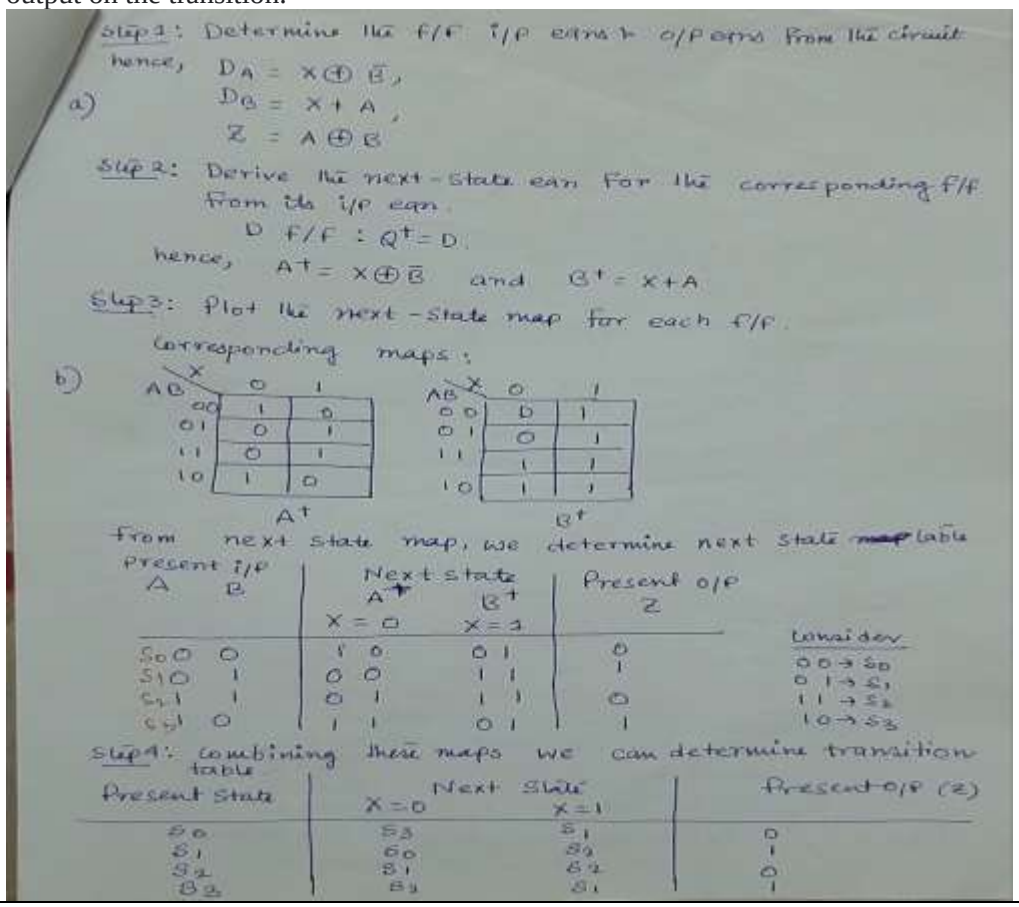
The gain of the DAC is decided by the (Rf/R) factor. For unity gain and in-phase output, we can use the buffer amplifier and perform the functions.

6	**Differentiate between Moore and Mealy machines. Analyze the following Moore sequential circuit for an input sequence X=01101 and draw a timing diagram.**



ANS:

A Mealy Machine changes its output on the basis of its present state and current input. A Moore Machine's output depends only on the current state. It does not depend on the current input. Mealy Machine places its output on the transition.



Step 1: Determine the f/f i/p eqns & o/p eqns from the circuit

hence, $D_A = X \oplus \bar{B}$,

a) $D_B = X + A$,

$Z = A \oplus B$

Step 2: Derive the next-state eqn for the corresponding f/f from its i/p eqn.

D f/f : $Q^+ = D$

hence, $A^+ = X \oplus \bar{B}$ and $B^+ = X + A$

Step 3: Plot the next-state map for each f/f.

Corresponding maps:

b)

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

A^+

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

B^+

from next state map, we determine next state table

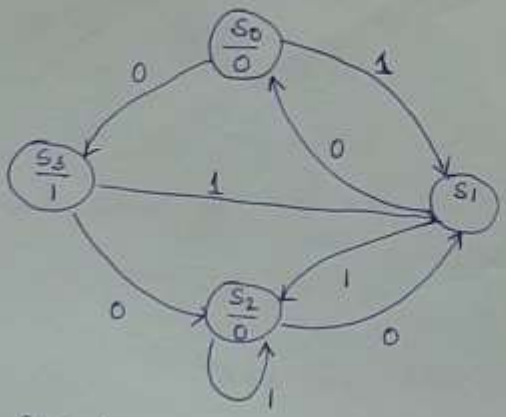
Present i/p A	Present i/p B	Next state A^+ X=0	Next state A^+ X=1	Next state B^+ X=0	Next state B^+ X=1	Present o/p Z
S_0 0	0	1	0	0	1	0
S_1 0	1	0	0	1	1	1
S_2 1	1	0	1	1	1	0
S_3 1	0	1	1	0	1	1

Consider
$00 \rightarrow S_0$
$01 \rightarrow S_1$
$11 \rightarrow S_2$
$10 \rightarrow S_3$

Step 4: combining these maps we can determine transition table

Present State	Next State X=0	Next State X=1	Present o/p (Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_3	S_1	1

State graph



c) Input sequence X = 01101

assumption:

I) Initial or state is A = 0, B = 0

II) All state changes occur after rising (active) edge of the clock.

III) I/P Seq. X is synchronized with the clock. Therefore, the system assumes its next state value after each rising edge of clock signal.

IV) O/P Z is a function of the present state i/p i.e., $Z = A \oplus B$, hence, the O/P will change when the state changes.

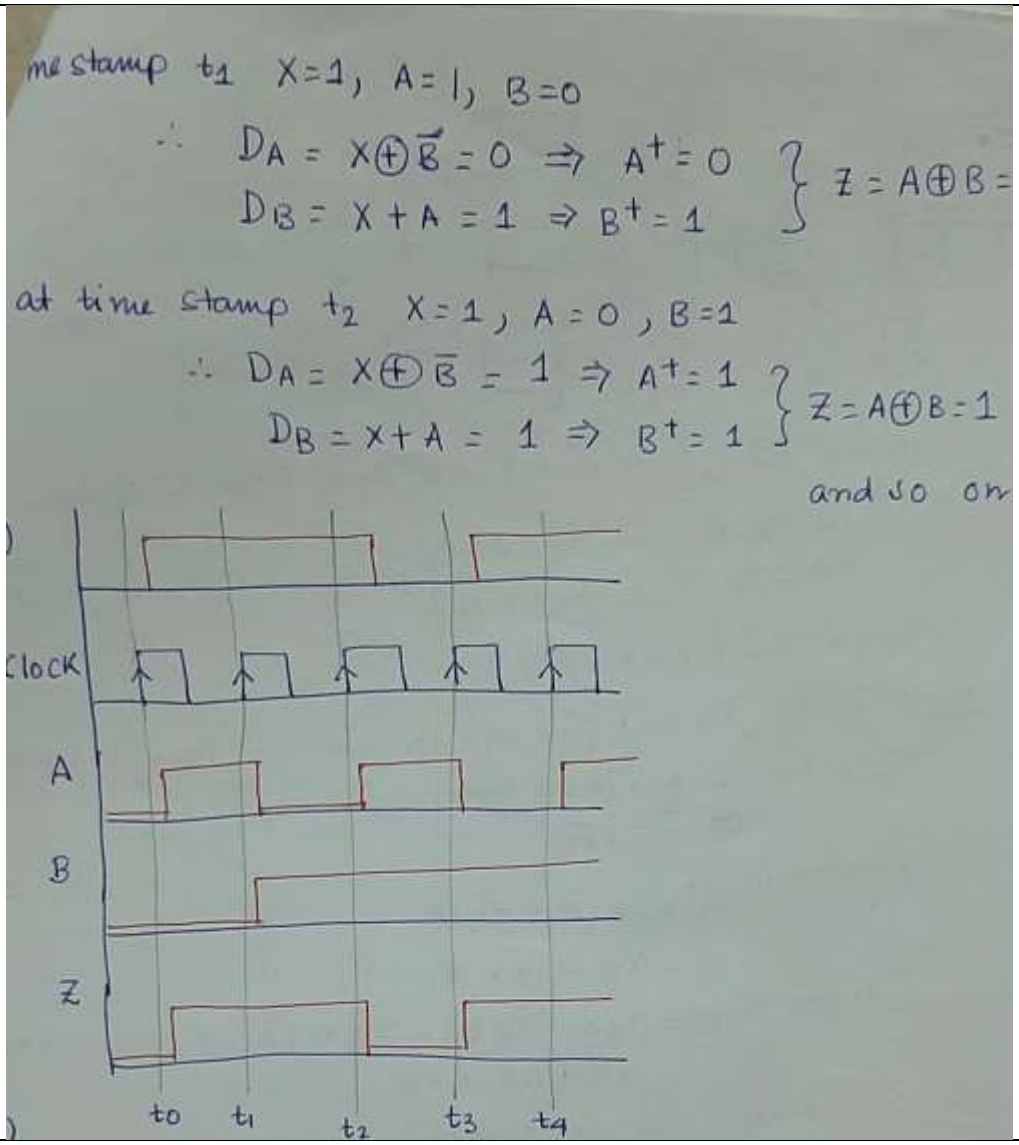
Operation:

X =	0	1	1	0	1	
A =	0	1	0	1	0	1
B =	0	0	1	1	1	1
Z =	(0)	1	1	0	1	(0)

at time t_0, $X=0, A=0, B=0 \Rightarrow D_A = X \oplus \bar{B} = 1$

So O/P of DFF A $\Rightarrow A^+ = 1$

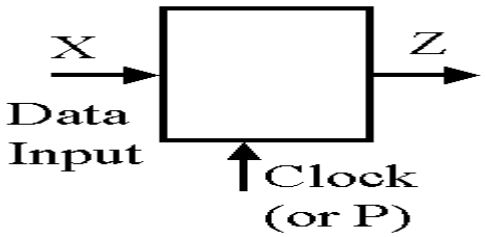
and $D_B = A + X$ O/P of DFF B $\Rightarrow B^+ = 0$ } $Z = A \oplus B = 0$



7 **With the help of state graph, state and transition tables and timing diagram explain sequential working principle of parity checker.**

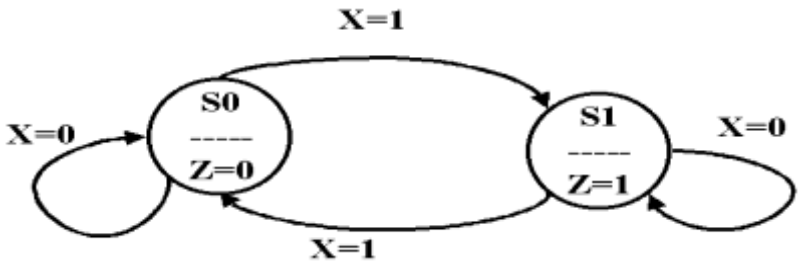
ANS: Consider : a **sequential** parity checker

- an 8th bit is added to each group of 7 bits such that the total # of 1 bits is odd for odd parity
- if any odd # of bits in the 8 bit block changes value then the presence of this error can be detected
- we'll design a parity checker for serial data:



- first generate a **state graph**
  - S0: even number of 1's received so far

- S1: odd number of 1's received so far

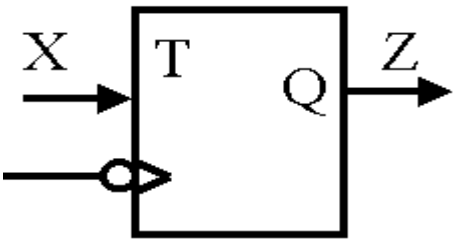


generate the **state table**

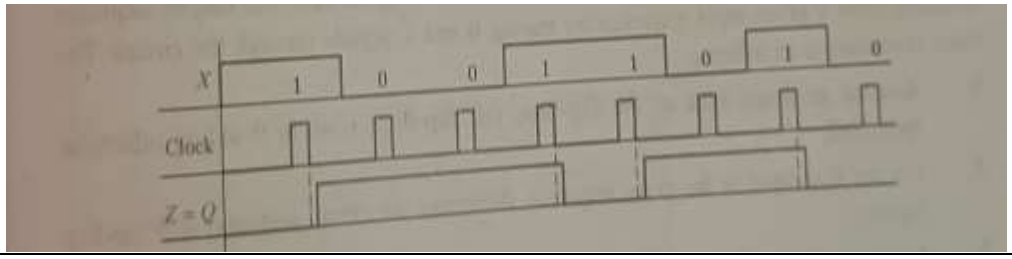
State Table		
X : input	Present State	Next State
0	S0	S0
1	S0	S1
0	S1	S1
1	S1	S0

- Since we only have two states, one bit will be used (or a single flipflop)
- We set up a table showing the next state as a function of the present state and the value of the current input signal X. We will use a T flip flop

X	Q	Q+	T
0	0	0	0
1	0	1	1
0	1	1	0
1	1	0	1



Timing diagram



	Above fig shows the output waveform for the circuit when X=1 the flip flop changes state after the falling edge of the clock .final value of Z is 0 ld be 1.because an even number of 1s was received . if the number of 1s received had been odd ,the final value of Z would be 1 .

Course Outcomes		Modules covered	PO1	PO2	PO3	PO4	PO5	PO6		PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	Design and analyze application of analog circuits using photo devices, timer IC, power supplyand regulator IC and op-amp.	1	2	3	3	2	2	0	0	0	0	0	0	0	0	2	0	2	2
CO2	Explain the basic principles of A/D and D/A conversion circuits and develop the same	1	2	2	3	2	2	0	0	0	0	0	0	0	0	2	0	2	2
CO3	Simplify digital circuits using Karnaugh Map , and Quine-McClusky Methods	2	2	3	3	3	2	0	0	0	0	0	0	0	0	2	0	2	2
CO4	Explain Gates and flip flops and make us in designing different data processing circuits, registers and counters and compare the types.	3, 4, 5	2	3	3	3	3	0	0	0	0	0	0	0	0	2	0	2	2
CO5	Develop simple HDL programs	3, 4, 5	1	1	1	1	3	0	0	0	0	0	0	0	0	2	0	2	1

COGNITIVE LEVEL	REVISED BLOOMS TAXONOMY KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PROGRAM OUTCOMES (PO), PROGRAM SPECIFIC OUTCOMES (PSO)				CORRELATION LEVELS	
PO1	Engineering knowledge	PO7	Environment and sustainability	0	No Correlation
PO2	Problem analysis	PO8	Ethics	1	Slight/Low
PO3	Design/development of solutions	PO9	Individual and team work	2	Moderate/ Medium
PO4	Conduct investigations of complex problems	PO10	Communication	3	Substantial/ High
PO5	Modern tool usage	PO11	Project management and finance		
PO6	The Engineer and society	PO12	Life-long learning		
PSO1	Develop applications using different stacks of web and programming technologies				
PSO2	Design and develop secure, parallel, distributed, networked, and digital systems				
PSO3	Apply software engineering methods to design, develop, test and manage software systems.				
PSO4	Develop intelligent applications for business and industry				