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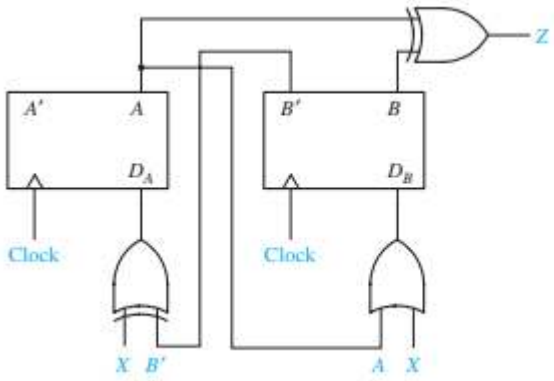
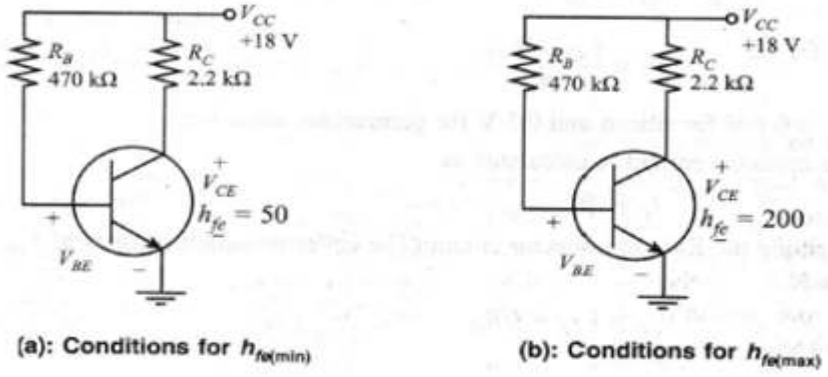
CMRIT — CMR INSTITUTE OF TECHNOLOGY, BENGALURU. ACCREDITED WITH A+ GRADE BY NAAC

Internal Assessment Test 3 – March 2022

Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	ISE
Date:	08/3/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A, B and C	OBE	

Answer any FIVE FULL Questions

			MARKS	CO	RBT
1		With a neat diagram, explain the working principle of photocoupler and mention its applications.	10	CO1	L1
2		Construct Mod 5 counter using SR flip flops	10	CO4	L3
3		With a neat waveform and circuit diagram, explain the working of monostable multivibrator.	10	CO1	L2
4	a	List the different types of BJT biasing. Derive the expression for collector emitter voltage (V_{CE}) for collector to base bias circuit.	6	CO1	L2
	b	Explain Successive Approximation Analog to Digital Converter.	4	CO2	L2
5		Analyze the following Moore Sequential circuit for an input sequence of X = 01101 and draw the timing diagram 	10	CO4	L3
6	a	Explain the working of R-2R ladder Digital to Analog Converter	5	CO2	L2
	b	Calculate the maximum and minimum levels of I_C and V_{CE} for the base bias circuit shown below, when h_{fe} = 50 and h_{fe} = 200 	5	CO1	L3

Faculty Signature CCI Signature HOD Signature

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CMRIT
CELEBRATING 25 YEARS
CMR INSTITUTE OF TECHNOLOGY, BENGALURU.
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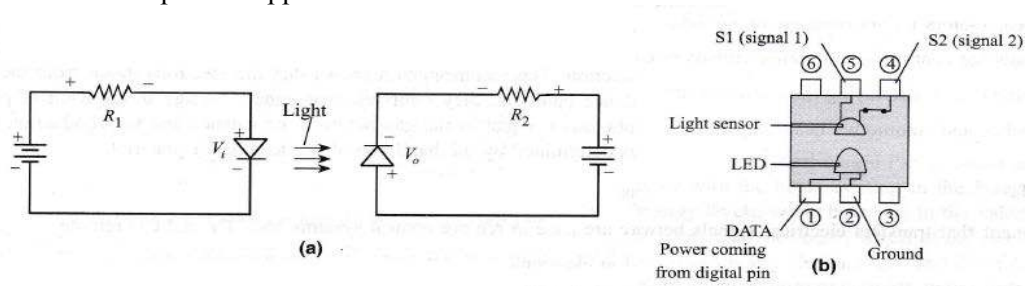
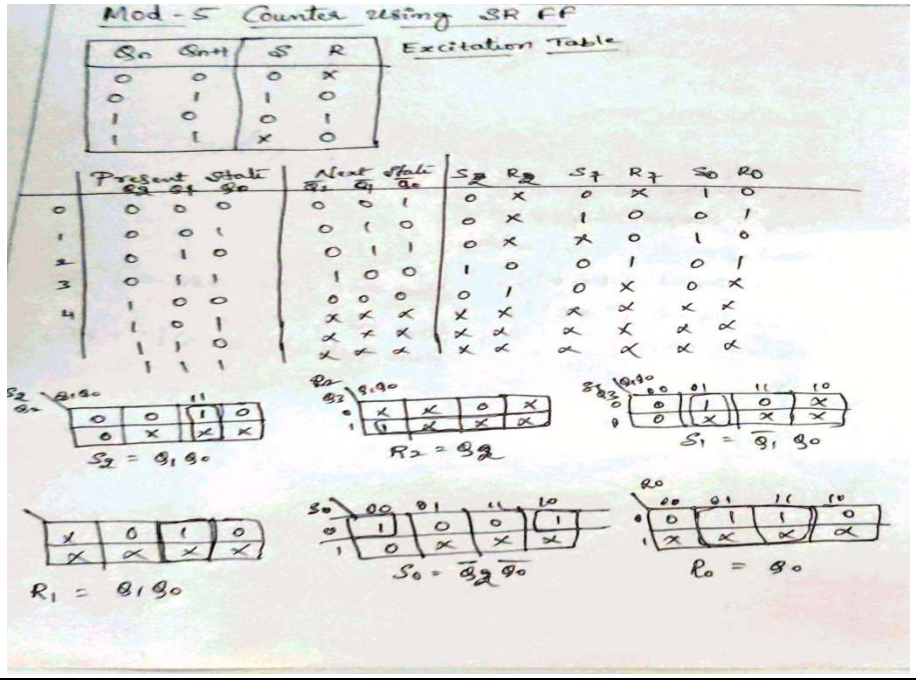
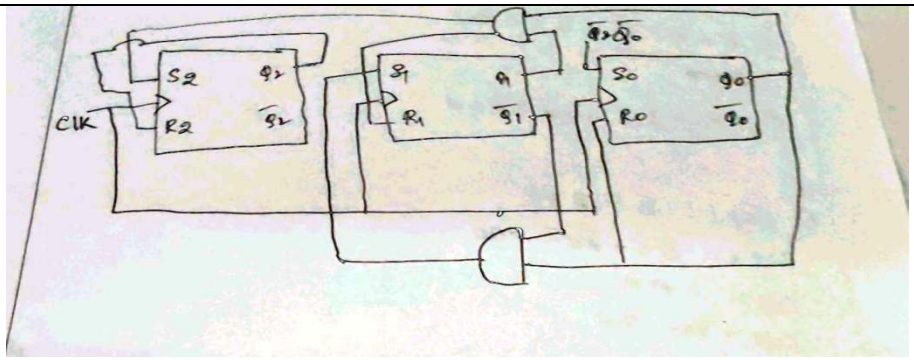
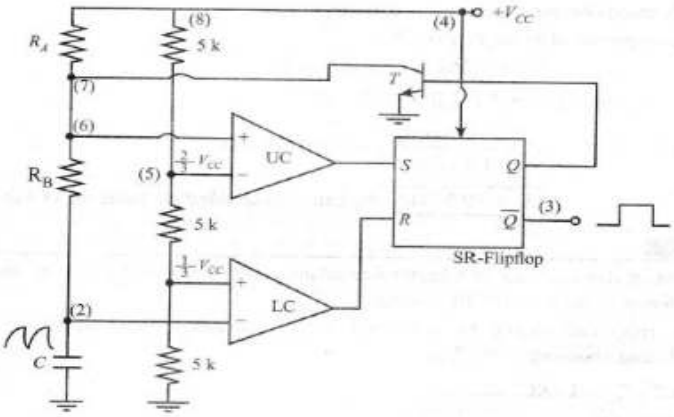
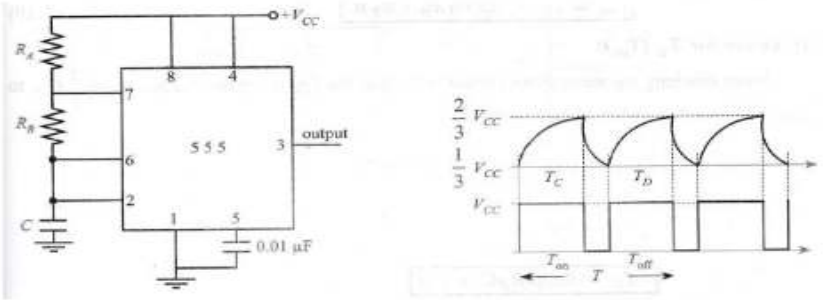
Internal Assessment Test 3 – March 2022

Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	ISE
Date:	7/3/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A, B and C		OBE

Answer any FIVE FULL Questions

		MARKS	CO	RBT
1	With a neat diagram, explain the working principle of photo-coupler and mention its applications. **Solution:** Construction: All photo-couplers consist of two elements: a light source (a LED) and a photo sensor (a photo resistor, photodiode, phototransistor, silicon-controlled rectifier (SCR), or triac); which are separated by a dielectric (non-conducting) barrier. Working Principle: When input current is applied to the LED, it switches ON and emits infrared light; the photo sensor then detects this light and allows current to flow through the output side of the circuit; conversely, when the LED is off, no current will flow through the photo sensor. By this method, the two flowing currents are electrically isolated. It consists of LED and photodiode; where the circuits are isolated electrically. In the following Figure, LED is forward biased, photodiode is reverse biased and output exists across R2. Applications: • Input and output switching in electronically noisy environments. • Controlling transistors and triacs. •Switch-mode power supplies 	10	CO1	L1
2	Construct Mod 5 counter using SR flip flops **Solution:** 	10	CO4	L3

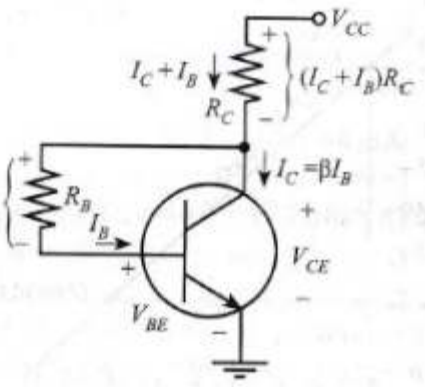
				
3	With a neat waveform and circuit diagram, explain the working of monostable multivibrator. **Solution:** An astable multivibrator does not have any stable state; it keeps changing its state from low to high and high to low**.**   **ON time operation:** o At $t = 0$, the voltage on the capacitor $V_{CC} = 0$, the same capacitor voltage is applied to both trigger point of lower comparator and threshold point of upper comparator. As capacitor voltage $V_C = 0$, which is less $1/3\ V_{CC}$, the output of lower comparator goes high ($\bar{Q} = 1$) and $Q = 0$. This causes T to go off and capacitor starts charging through series resistors R_A and R_B. When capacitor voltages reaches $2/3\ V_{CC}$, on time is terminated. **OFF time operation:** o As soon as V_C exceeds $2/3\ V_{CC}$, the upper comparator output goes high and it will set the SR FF. i.e., $S = 1$ and $R = 0$ and $Q = 1$ and $\bar{Q} = 0$. This will turn on transistor T, and output at pin (3) goes low. o Now, the capacitor discharges through R_B, and through transistor T. The discharge time (also called off time (T_D); and it depends on the values of R_B and C. When capacitor voltage is $V_C = 1/3\ V_{CC}$, lower comparator output goes high.	5	CO1	L2
4a	List the different types of BJT biasing. Derive the expression for collector emitter voltage (V_{CE}) for collector to base bias circuit.	5	CO1	L2

Solution:

The different types of BJT biasing are

1. Fixed Bias 2. Collector to Base Bias 3. Voltage Divider Bias

Collector to base bias



Applying KVL to the outer loop;

$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$ Or, $V_{CE} = V_{CC} - (I_C + I_B) R_C$ ----------

Applying KVL to the loop V_{CE}, I_BR_B, and V_{BE};

$V_{CE} - V_{BE} - I_BR_B = 0$ Or, $V_{CE} = V_{BE} + I_BR_B$ ----------

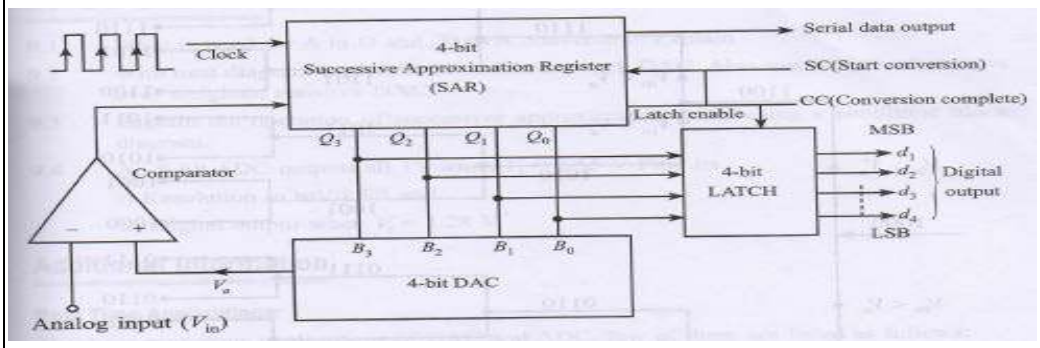
Equating equations 3a and 3b;

$V_{CC} - (I_C + I_B) R_C = V_{BE} + I_BR_B$

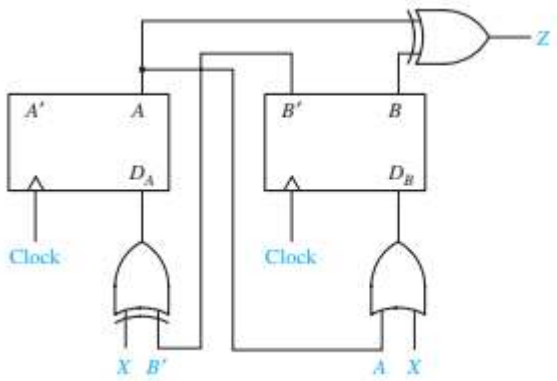
Or, $(I_C + I_B) R_C + I_BR_B = V_{CC} - V_{BE}$ i.e., $I_B (R_C + R_B) + I_CR_C = V_{CC} - V_{BE}$

Substituting $I_C = \beta I_B$ in above equation, we get;

$I_B (R_C + R_B) + \beta I_BR_C = V_{CC} - V_{BE}$ Gives, $I_B = (V_{CC} - V_{BE})/(\beta+1)R_C + R_B$ ----------

4b	Explain Successive Approximation Analog to Digital Converter. **Solution:**  Figure shows a successive approximation register (SAR), the output of which is connected to DAC and output latch circuit. The input signal (Vin) is compared with the analog output signal (Va) of the DAC. Output of the comparator is feedback into SAR. The control logic inside SAR adjusts its digital output; until it is equal to the analog input signal. At the start of conversion cycle, start conversion terminal is made high. On the first clock pulse, the output of the SAR is made 1000. The DAC produces an analog voltage (Va) proportional to 1000. This analog voltage is compared with input analog signal (Vin). If Vin > Va, the comparator output will be high and SAR keeps Q3 high. On the other hand, if Vin < Va, then the comparator output becomes low and SAR resets Q3 to low. If Vin > Va, SAR follows the upward path in code tree and if Vin < Va, SAR follows downward path.	5	CO2	L2

5	Analyze the following Moore Sequential circuit for an input sequence of X = 01101 and draw the timing diagram	10	CO4	L3



Solution:

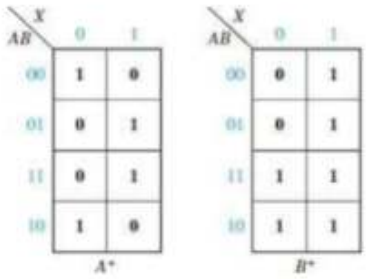
1. The flip-flop input equations and output equation are

$$D_A = X \oplus B' \qquad D_B = X + A \qquad Z = A \oplus B$$

2. The next-state equations for the flip-flops are

$$A^+ = X \oplus B' \qquad B^+ = X + A$$

3. The corresponding maps are



(a)

AB	A^+B^+ X = 0	X = 1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

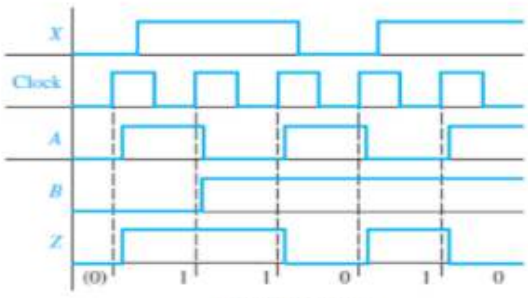
(b)

Present State	Next State X = 0	X = 1	Present Output (Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

State Tables

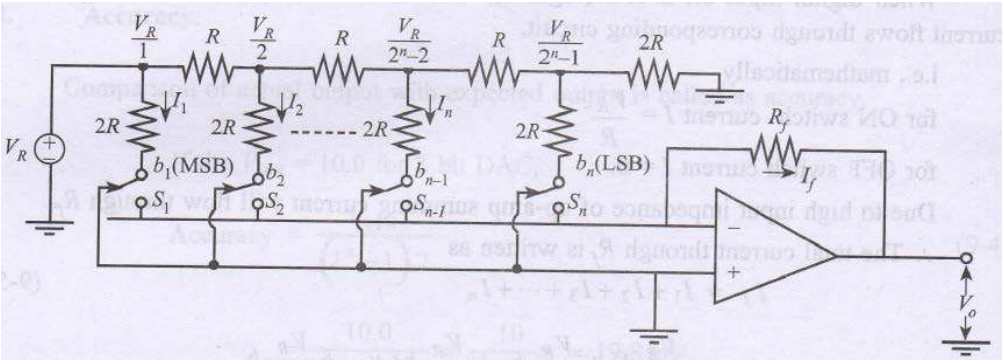
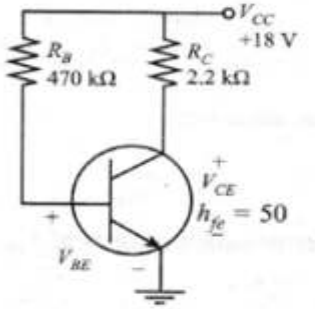
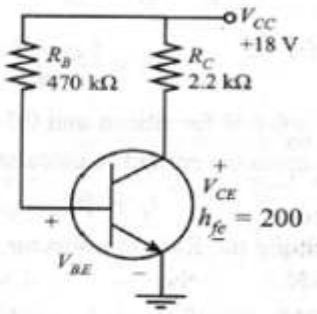
4. Combining these maps yields the transition table (Table (a)), which gives the next state of both flip-flops (A^+B^+) as a function of the present state and input. The output function Z is then added to the table. In this example, the output depends only on the present state of the flip-flops and not on the input, so only a single output column is required.

Using the above Table (a), we can construct the timing chart for some given input sequence and specified initial state.



Timing Chart

Initially AB = 00 and X = 0, so Z = 0 and A^+B^+ = 10. This means that after the rising clock edge, the flip-flop state will be AB = 10. Then, with AB = 10, the output is Z = 1. The next input is X = 1, so A^+B^+ = 01 and the state will change after the next rising clock edge. Continuing in this manner, we can complete the timing chart.

6	a. Explain the working of R-2R ladder Digital to Analog Converter. **Solution:**  Each binary bit connects switch either to ground (non-inverting input) or to the inverting terminal of Op-Amp. Due to virtual ground, both the positions of the switches are at ground potential, and currents through the resistances are constant. The current flowing through each of 2R resistances; $I_1 = \frac{V_R}{2R}$ $I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R}$ $I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R}$ $I_n = \frac{V_R/(2^n-1)}{2R}$ But, $V_0 = -I_f R_f = -R_f(I_1 + I_2 + \ldots + I_N)$ $i.e., V_0 = -R_f\left[\frac{V_R}{2R}b_1 + \frac{V_R}{4R}b_2 + \ldots + \frac{V_R}{2^n R}b_n\right]$ Or, $V_0 = -\frac{V_R}{R}R_f[b_1 2^{-1} + b_2 2^{-2} + \ldots + b_n 2^{-n}]$ If $R_f = R$; $\boldsymbol{V_0 = -V_R[b_1 2^{-1} + b_2 2^{-2} + \ldots + b_n 2^{-n}]}$	5	CO2	L2
	b. Calculate the maximum and minimum levels of I_C and V_{CE} for the base bias circuit shown below, when $h_{fe} = 50$ and $h_{fe} = 200$  (a): Conditions for $h_{fe(min)}$  (b): Conditions for $h_{fe(max)}$ **Solution:** Given: $h_{fe(min)} = 50$, $h_{fe(max)} = 200$, $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 36.8\,\mu\text{A}$ **Case i:** $h_{fe(max)} = 200$ $I_C = h_{fe} I_B = 200 \times 36.8\,\mu\text{A} = 7.36\text{ mA}$ $V_{CE} = V_{CE} - I_C R_C = 18\text{ V} - (7.36\text{ mA} \times 2.2\text{ k}\Omega) = 1.8\text{ V}$ **Case ii:** $h_{fe(min)} = 50$ $I_C = h_{fe} I_B = 50 \times 36.8\,\mu\text{A} = 1.84\text{ mA}$ $V_{CE} = V_{CE} - I_C R_C = 18 - (1.84\text{ mA} \times 2.2\text{ k}\Omega) = 13.95\text{ V}$	5	CO1	L3