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Internal Assessment Test 1 – Nov. 2021 (Scheme & Solution)

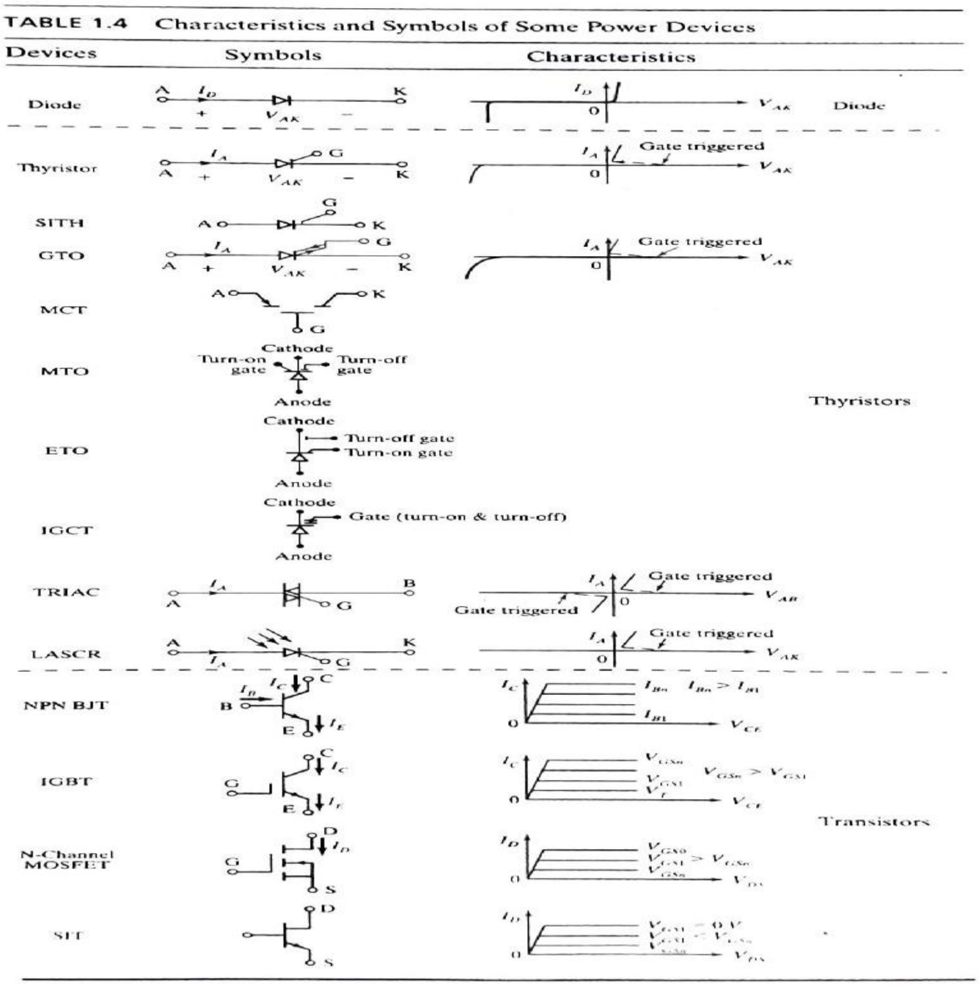
Sub:	POWER ELECTRONICS					Sub Code:	17EC73/ 15EC73	Branch:	ECE
Date:	13-11-2021	Duration:	90 mins (2pm-3.30pm)	Max Marks:	50	Sem/Sec:	VII E		OBE

Answer any FIVE FULL Questions | MARKS | CO | RBT

1 Give the characteristics features of following devices with symbols [10] CO1 L1

i) IGBT **ii)** TRIAC **iii)** MOSFET **iv)** MCT **v)** LASCR

Sol.



Each characteristics=1 mark, Each Symbol= 1 mark; 2*5=10 marks.

2 With a neat diagram and waveforms, explain the steady state characteristics of BJT. [10] CO1 L2

Soln.

- There are 3 possible configurations – Common Collector, Comm Base & Common Emitter.
- The Common Emitter, shown in Figure 4.28a for an NPN transist is generally used in switching applications.
- The typical input characteristics of base current I_B against ba emitter voltage V_{BE} are shown in Figure 4.28b.
- Figure 4.28c shows the typical output characteristics of collec current I_C against collector-emitter voltage V_{CE}.
- For a PNP-transistor, the polarities of all currents and voltages reversed.

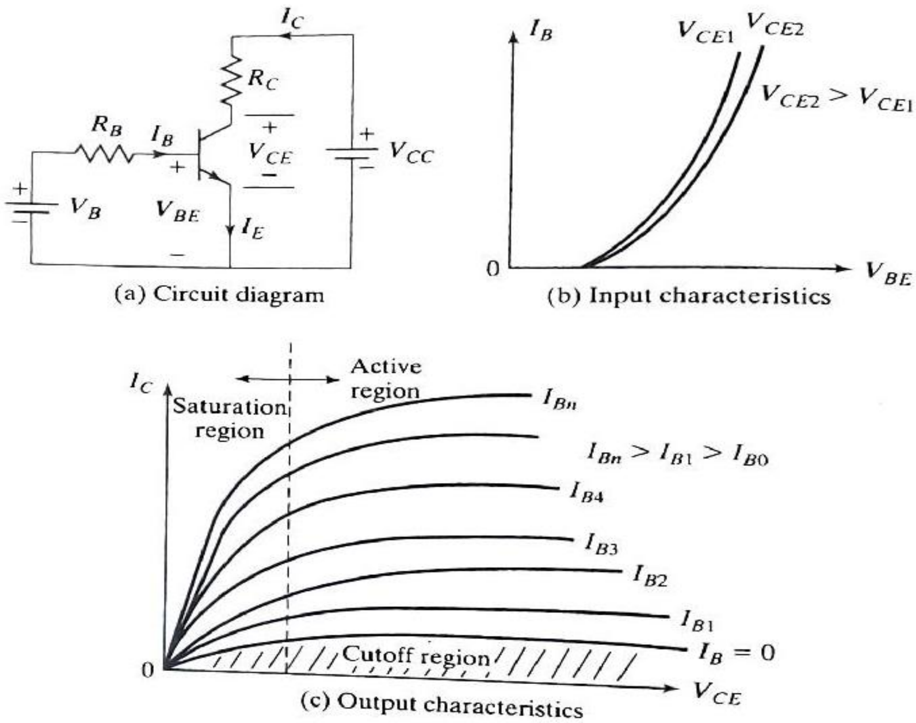


FIGURE 4.28

Characteristics of *NPN*-transistors.

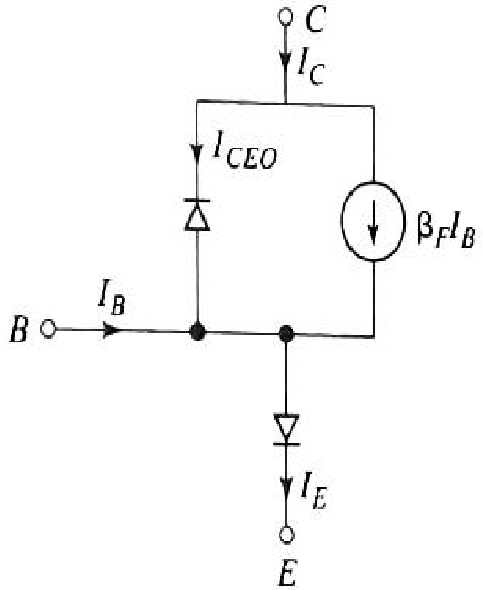


FIGURE 4.30
Model of *NPN*-transistors.

- There are 3 operating regions of a transistor : Cutoff, Active Saturation.
- In the cutoff region, the transistor is off.
- The base current is not enough to turn it on & hence b junctions are reverse biased.
- In the active region, the transistor acts as an amplifier, where base current is amplified by a gain.
- The collector-emitter voltage decreases with the base current.
- The CBJ (Collector to Base Junction) is reverse biased & the (Base to Emitter Junction) is forward biased.
- In the saturation region, the base current is sufficiently high.
- The collector-emitter voltage is low, & the transistor acts a switch.
- Both junctions (CBJ & BEJ) are forward biased.
- The transfer characteristic, which is a plot of V_{CE} against I_B shown in Figure 4.29.

- The model of an NPN transistor is shown in Figure 4.30 und large-signal dc operation.
- The equation relating the currents is

$I_E = I_C + I_B$ (4.14)

- The base current is effectively the input current & the collec current is the output current.
- The ratio of the collector current I_C to base current I_B is known the forward **current gain**, β_F :

$$\beta_F = h_{FE} = \frac{I_C}{I_B} \qquad (4.15)$$

• The collector current has 2 components : one due to base current & the other is the leakage current of the CBJ.	[10]	CO1	L1

$$I_C = \beta_F I_B + I_{CEO} \qquad (4.16)$$

- Where I_{CEO} is the collector-to-emitter leakage current with base open circuit & can be considered negligible compared to $\beta_F I_B$.
- From Eqs. (4.14) and (4.16), we have

$$I_E = I_B(1 + \beta_F) + I_{CEO} \quad (4.17)$$

$$\approx I_B(1 + \beta_F) \quad (4.18)$$

$$I_E \approx I_C\left(1 + \frac{1}{\beta_F}\right) = I_C \frac{\beta_F + 1}{\beta_F} \quad (4.19)$$

Because $\beta_F \gg 1$, the collector current can be expressed as

$$I_C \approx \alpha_F I_E \quad (4.20)$$

where the constant α_F is related to β_F by

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \quad (4.21)$$

or

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad (4.22)$$

Let us consider the circuit of Figure 4.31, where the transistor is operated as a switch.

$$I_B = \frac{V_B - V_{BE}}{R_B} \quad (4.23)$$

$$V_C = V_{CE} = V_{CC} - I_C R_C = V_{CC} - \frac{\beta_F R_C}{R_B}(V_B - V_{BE})$$

$$V_{CE} = V_{CB} + V_{BE} \quad (4.24)$$

or

$$V_{CB} = V_{CE} - V_{BE} \quad (4.25)$$

Figures & Waveforms= 5 marks, Explanation & Eqns.= 5 marks.

3 Draw the switching model of MOSFET and explain its switching characteristics with neat figure.

Soln.

- Without any gate signal, the enhancement-type MOSFET may be considered as 2 diodes connected back to back.
- This is similar to an NPN-transistor.
- The gate structure has parasitic capacitances to the source, C_{gs}, & to the drain, C_{gd}.
- The NPN-transistor has a reverse-bias junction from the drain to the source & offers a capacitance, C_{ds}.

Figure 4.8a shows the equivalent circuit of a parasitic bipolar transistor in parallel with a MOSFET.

The base-to-emitter region of an NPN-transistor is shorted at the chip.

This is done by metalizing the source terminal & the resistance from the base to emitter.

This is because the bulk resistance of n- and p- regions, Rbe, is small.

Hence, a MOSFET may be considered as having an internal diode & the equivalent circuit is shown in Figure 4.8b.

The parasitic capacitances are dependent on their respective voltages.

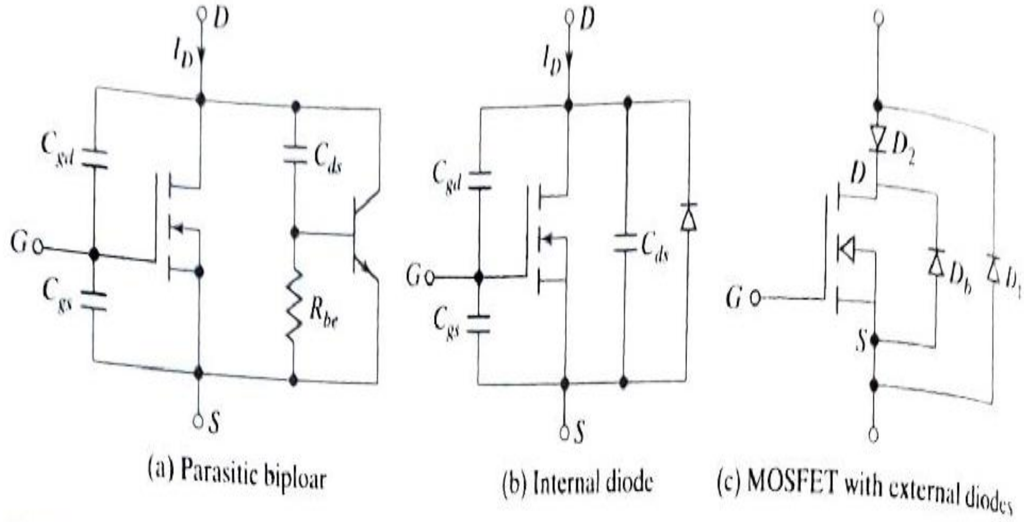


FIGURE 4.8

Parasitic model of enhancement of MOSFETs.

- The internal built-in diode is often called the **body diode**.
- The switching speed of the body diode is much slower than that of the MOSFET.
- Thus, an NMOS (n-channel metal oxide semiconductor) will behave as an uncontrolled device.
- As a result, a current can flow from the source to drain if the circuit conditions prevail for a negative current.
- This is true if the NMOS is switching power to an inductive load.
- In this case, the NMOS will act as a freewheeling diode & provide a path for current flow from the source to the drain.
- The NMOS will behave as an uncontrolled device in the reverse direction.

- The NMOS data sheet would normally specify the current rating of the parasitic diode.
- If the body diode D_b is allowed to conduct, then a high peak current can occur during the diode turn-off transition.
- Most MOSFETs are not rated to handle these currents, & device failure can occur.
- To avoid this situation, external series D_2 & antiparallel diodes D_1 can be added as in Figure 4.8c.

- Power MOSFETs can be designed to have a built-in fast-recovery body diode.
- Also, they can be designed to operate reliably when the body diode is allowed to conduct at the rated MOSFET current.

- However, the switching speed of such body diodes is still somewhat slow.
- This can result in significant switching loss due to diode stored charge.
- The designer should check the ratings & the speed of the body diode to handle the operating requirements.

The switching model of MOSFETs with parasitic capacitances is shown in Figure 4.9.

The typical switching waveforms & times are shown in Figure 4.10.

The turn-on delay td(on) is the time that is required to charge the input capacitance to threshold voltage level.

The rise time tr is the gate-charging time from the threshold level to the full-gate voltage VGSP.

This is required to drive the transistor into the linear region.

The turn-off delay time td(off) is the time required for the input capacitance to discharge from the overdrive gate voltage V1 to the pinch-off region.

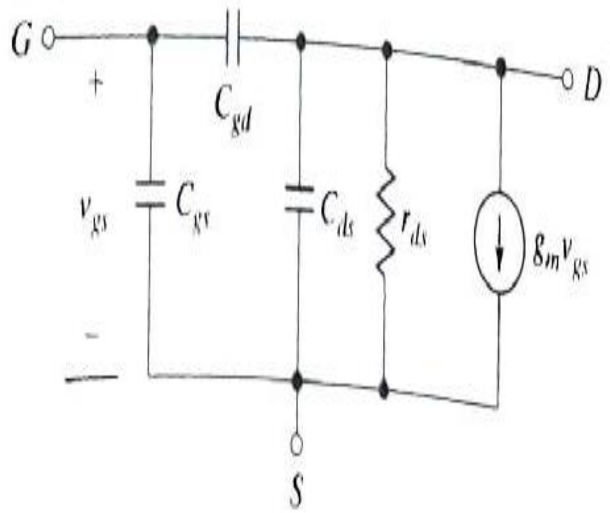


FIGURE 4.9

Switching model of MOSFETs.

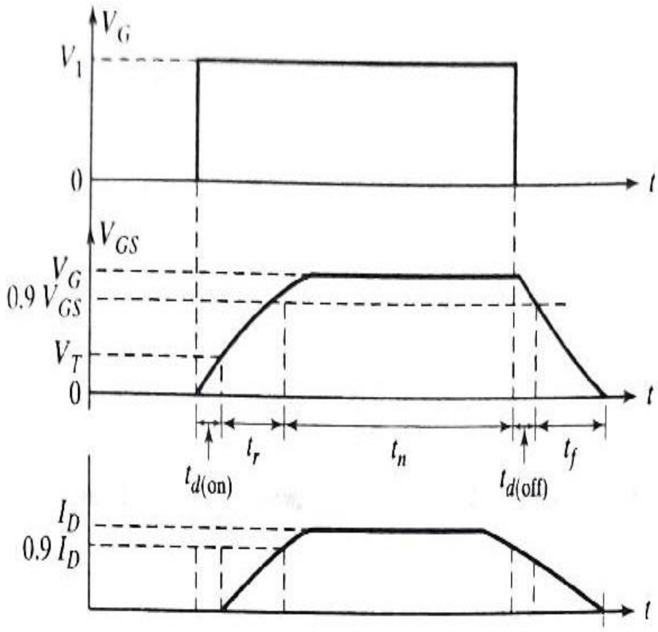


FIGURE 4.10
Switching waveforms and times.

- V_{GS} must decrease significantly before V_{DS} begins to rise.
- The **fall time t_f** is the time that is required for the input capacitance to discharge from the pinch-off region to threshold voltage.
- If $V_{GS} \le V_T$, the transistor turns off.

4	Mention and explain the different types of power electronic converter systems. Soln. • The power electronic circuits can be classified into 6 types : 1) Diode Rectifiers 2) DC-DC Converters (DC Choppers) 3) DC-AC Converters (Inverters) 4) AC-DC Converters (Controlled Rectifiers) 5) AC-AC Converters (AC Voltage Controllers) 6) Static Switches Each type – Fig. & Explanation = 10 marks.	[10]	CO1	L1
5	a) Define power electronics and mention its different applications. b) Explain operation of IGBT with neat circuit diagram and waveforms. Soln.	[05+05]	CO1	L1

a)

c) **Power Electronics** may be defined as the application of soli electronics for the control & conversion of electric power.

d) Also, it can be defined as the art of converting electrical energy one form to another in an **efficient**, **clean**, **compact** & **robust** r for the energy utilization to meet the desired needs.

e) The interrelationship of power electronics with power, electron control is shown in Figure 1.1.

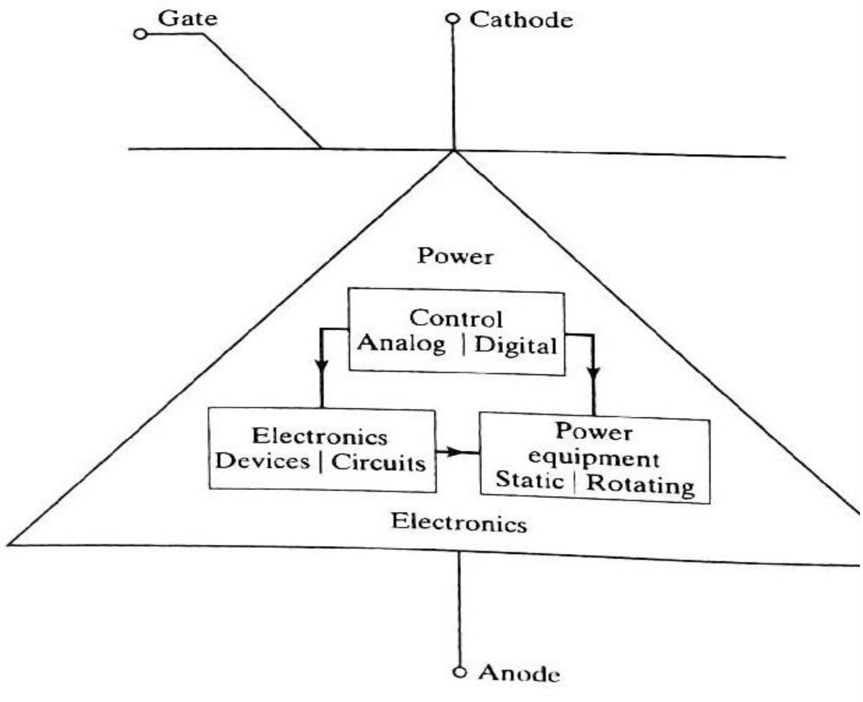


FIGURE 1.1

Relationship of power electronics to power, electronics, and control.

f) The arrow points to the direction of current flow from anode cathode (K).

g) It can be turned on & off by a signal to the gate terminal (G).

h) Without any gate signal, it normally remains in the off-state, beha an open circuit, and can withstand a voltage across the terminals K.

i) Power electronics has revolutionized the concept of power control

j) Power control is used for power conversion and for control of ele motor drives.

k) For many years, there was demand for control of electric power.

l) This electric power was to be used for motor drive system industrial controls.

m) This demand gave rise to early development of the Ward-L system.

n) The Ward-Leonard system is used to obtain a variable dc voltage control of dc motor drives.
(5 marks)

o) The operations of the power converters are based mainly o switching of power semiconductor devices.
p) This introduces current & voltage harmonics into the supply sys on the output of the converters.
q) These can cause problems of :
r) Distortion of the output voltage
s) Harmonic generation into the supply system
t) Interference with the communication & signaling circuits.
u) It is normally necessary to introduce filters on the input & outpu converter system.
v) This reduces the harmonic level to an acceptable magnitude.
w) Figure 1.11 shows the block diagram of a generalized power conv
x) The application of power electronics to supply the sensitive elec loads poses a challenge on the power quality issues.
y) The input & output quantities of converters could be either ac or d
z) Factors which are measures of the quality of a waveform are,
aa) Total Harmonic Distortion (THD).
bb) Displacement Factor (DF).
cc) Input Power Factor (IPF).
dd) To determine these factors, finding the harmonic content waveforms is required.
ee) To evaluate the performance of a converter, the input & voltages & currents of a converter are expressed in a Fourier series
ff) The quality of a power converter is judged by the quality of its v & current waveforms.
gg) The control strategy for the power converters plays an imp part on the harmonic generation & output waveform distortion.
hh) This control strategy can be aimed to minimize or reduce problems.
ii) The power converters can cause radio-frequency interference o electromagnetic radiation.
jj) This causes gating circuits to generate erroneous signals.
kk) This interference can be avoided by **grounded shielding**.

b)

- An IGBT combines the advantages of BJTs & MOSFETs.
- An IGBT has high input impedance, like MOSFETs, and low on-state conduction losses, like BJTs.
- However, there is no second breakdown problem, as with BJTs.
- By chip design & structure, the equivalent drain-to-source resistance R_{DS} is controlled to behave like that of a BJT.

- The silicon cross section of an IGBT is shown in Figure 4.39a, which is identical to that of an MOSFET except for the p^+ substrate.
- The performance of an IGBT is closer to that of a BJT than an MOSFET.
- This is due to the p+ substrate, which is responsible for the minority carrier injection into the n-region.
- The equivalent circuit is shown in Figure 4.39b, which can be simplified to Figure 4.39c.

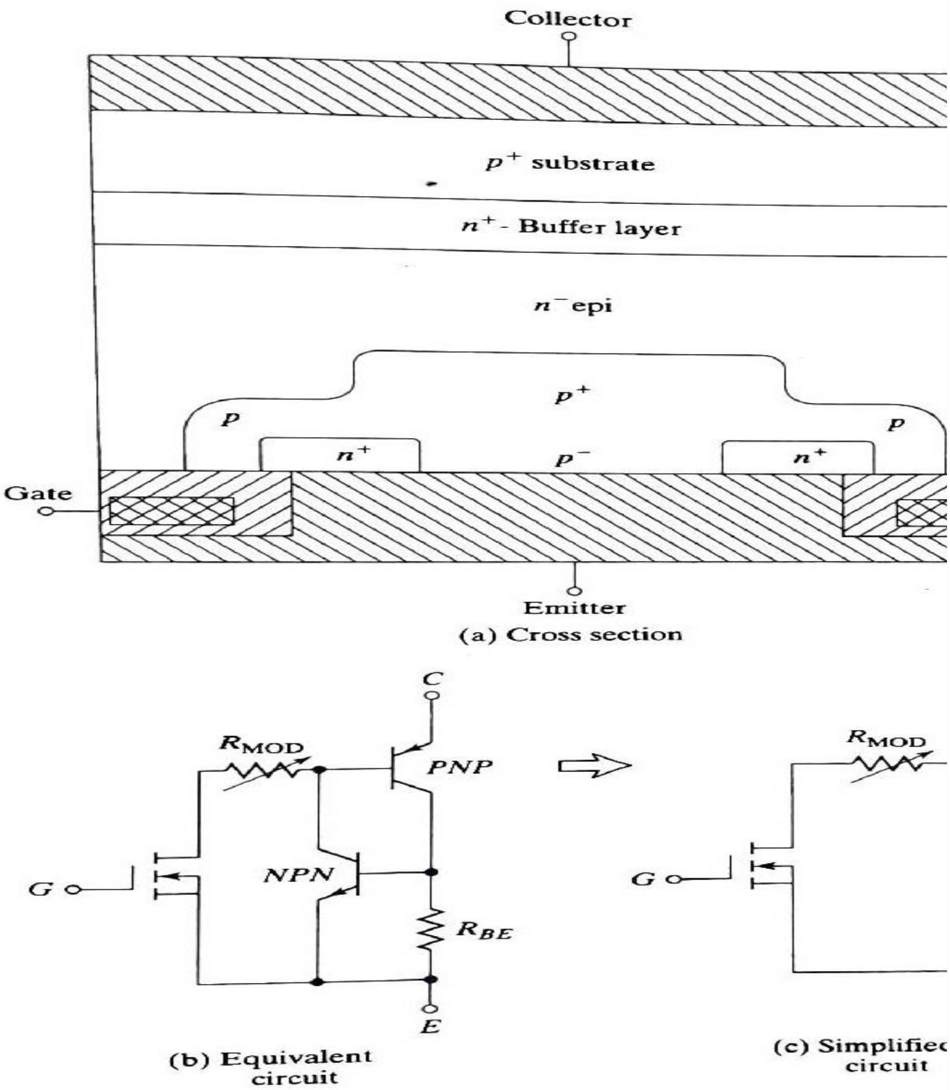


FIGURE 4.39
Cross section and equivalent circuit for IGBTs.

6	a) Explain di/dt and dv/dt limitations. b) With neat diagrams & explanation, differentiate between depletion and enhancement type MOSFETs.	[10]	CO1	L2

Soln.

a)

a) Transistors require certain turn-on & turn-off times.
b) Neglecting the delay time td and the storage time ts, the typical voltage & current waveforms of a transistor switch are shown in Figure 4.46.

c) During turn-on, the collector current rises and the di/dt is

$$\frac{di}{dt} = \frac{I_L}{t_r} = \frac{I_{cs}}{t_r} \quad (4.51)$$

d)

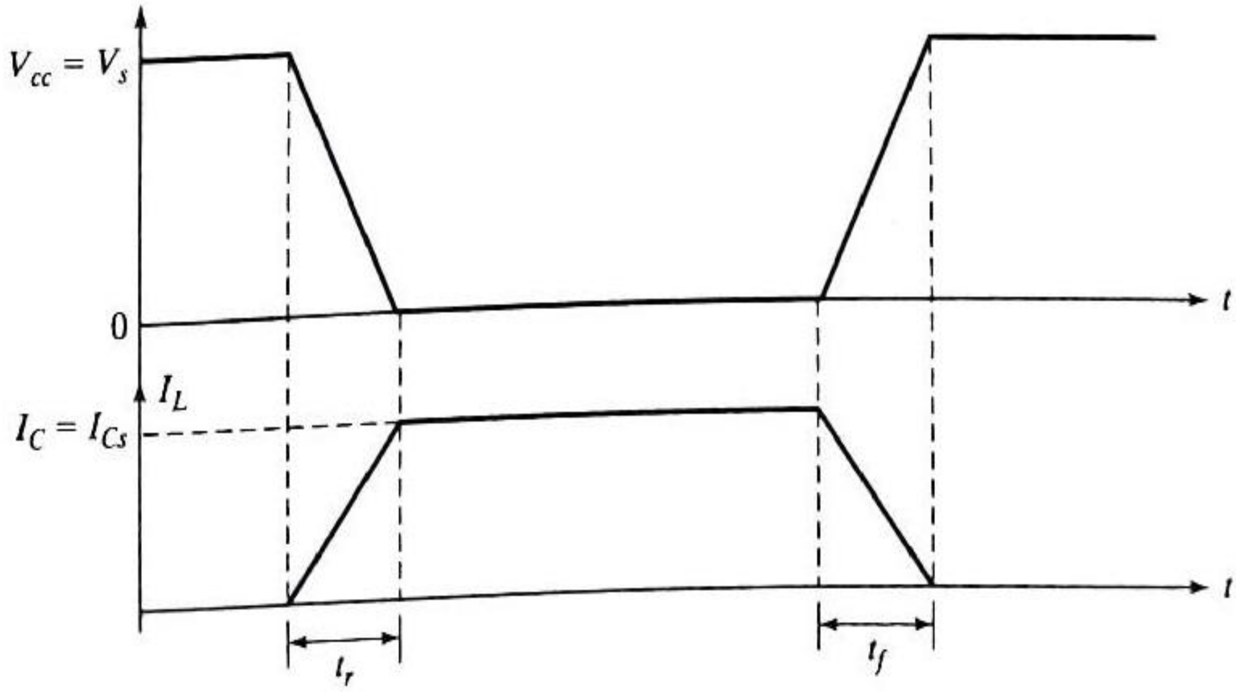


FIGURE 4.46

Voltage and current waveforms.

- During turn-off, the collector-emitter voltage must rise in relation to the fall of the collector current, and dv/dt is

$$\frac{dv}{dt} = \frac{V_s}{t_f} = \frac{V_{cs}}{t_f} \quad (4.52)$$

- The conditions di/dt and dv/dt in Eqs. (4.51) and (4.52) are set by the transistor switching characteristics.
They must be satisfied during turn-on and turn-off.
Protection circuits are normally required to keep the operating di/dt & dv/dt within the allowable limits of the transistor.
A typical transistor switch with di/dt & dv/dt protection is shown in Figure 4.47a, with the operating waveforms in Figure 4.47b.
The RC network across the transistor is known as the snubber circuit, or snubber, and limits the dv/dt.
The inductor Ls, which limits the di/dt, is sometimes called a series snubber.

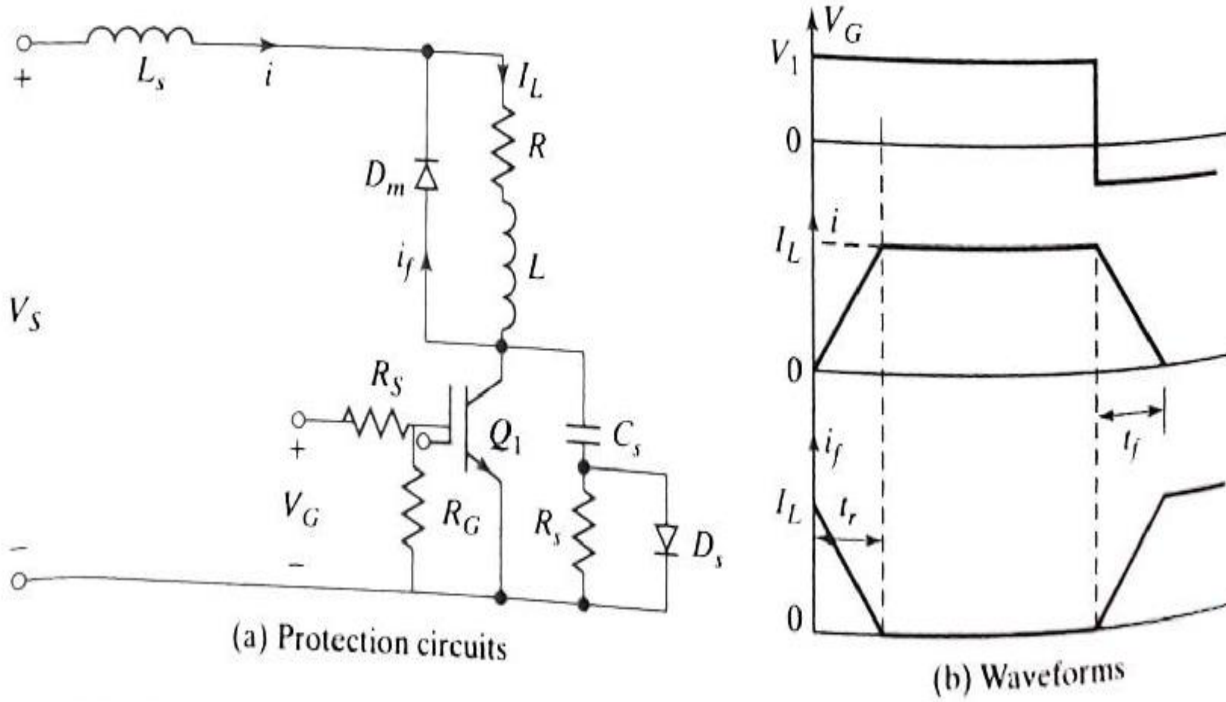


FIGURE 4.47

Transistor switch with di/dt and dv/dt protection.

-
  - Let us assume that under steady-state conditions, the load current IL is free wheeling through diode Dm.
  - Diode Dm is assumed to have negligible reverse recovery time.
  - When transistor Q1 is turned on, the collector current rises and current of diode Dm falls.
  - This is because Dm behaves as a short-circuit.
- The equivalent circuit during turn-on is shown in Figure 4.48a and turn-on di/dt is

$$\frac{di}{dt} = \frac{V_s}{L_s} \qquad (4.53)$$

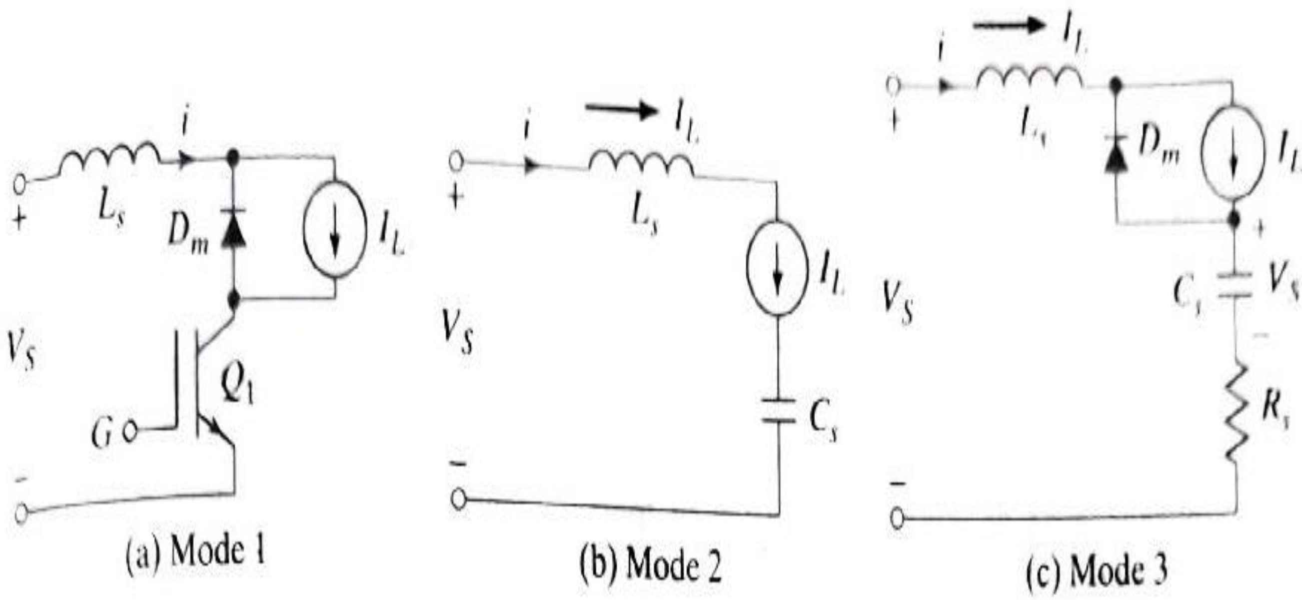


FIGURE 4.48

Equivalent circuits.

- Equating Eq.(4.51) to Eq.(4.53) gives the value of L_s,

$$L_s = \frac{V_s t_r}{I_L} \qquad (4.54)$$

During turn-off, the capacitor Cs charges by the load current & the equivalent circuit is shown in Figure 4.48b.
The capacitor voltage appears across the transistor and the dv/dt is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \qquad (4.55)$$

Equating Eq.(4.52) to Eq.(4.55) gives the required value of capacitance,

$$C_s = \frac{I_L t_f}{V_s} \qquad (4.56)$$

Once the capacitor is charged to Vs, the free wheeling diode turns on.
Due to the energy stored in Ls, there is a damped resonant circuit as shown in Figure 4.48c.

The transient analysis of RLC circuit is discussed in Section 17.4.
The RLC circuit is normally made critically damped to avoid oscillations.
For unity critical damping, δ=1, and Eq.(17.15) yields
δ = α/ω0 = (R/2)[(C/L)^0.5]   (17.15)

$$R_s = 2\sqrt{\frac{L_s}{C_s}} \tag{4.57}$$

The capacitor Cs has to discharge through the transistor & this increases the peak current rating of the transistor.
The discharge through the transistor can be avoided by placing resistor Rs across Cs instead of placing Rs across Ds.
The discharge current is shown in Figure 4.49.
When choosing the value of Rs, the discharge time, RsCs = τs should also be considered.
A discharge time of one-third the switching period Ts is usually adequate.

$$3R_sC_s = T_s = \frac{1}{f_s}$$

or

$$R_s = \frac{1}{3f_sC_s} \tag{4.58}$$

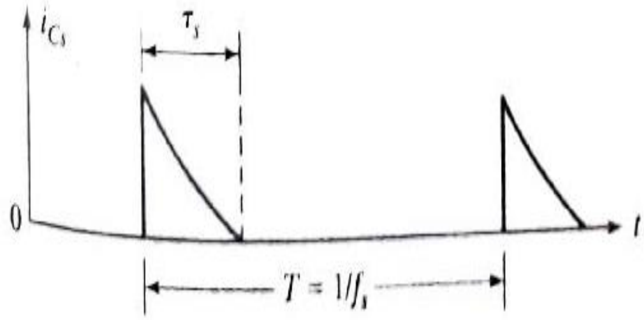


FIGURE 4.49
Discharge current of snubber capacitor.

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b)

- A power MOSFET is a voltage-controlled device and requires only a small input current.
- The switching speed is very high and the switching times are of the order of nanoseconds.
- Power MOSFETs find increasing applications in low-power high-frequency converters.
- MOSFETs do not have the problems of second breakdown phenomena as do BJTs.
- But, MOSFETs have the problems of electrostatic discharge & require special care in handling.
- In addition, it is relatively difficult to protect them under short-circuited fault conditions.

- The 2 types of MOSFETs are :

1) Depletion MOSFETs and
2) Enhancement MOSFETs

- An n-channel depletion-type MOSFET is formed on a p-type silicon substrate as shown in Figure 4.1a.
- It has 2 heavily doped n+ silicon sections for low resistance connections.
- The gate is isolated from the channel by the thin oxide layer.
- The 3 terminals are called **gate**, **drain**, & **source**.
- The substrate is normally connected to the source.

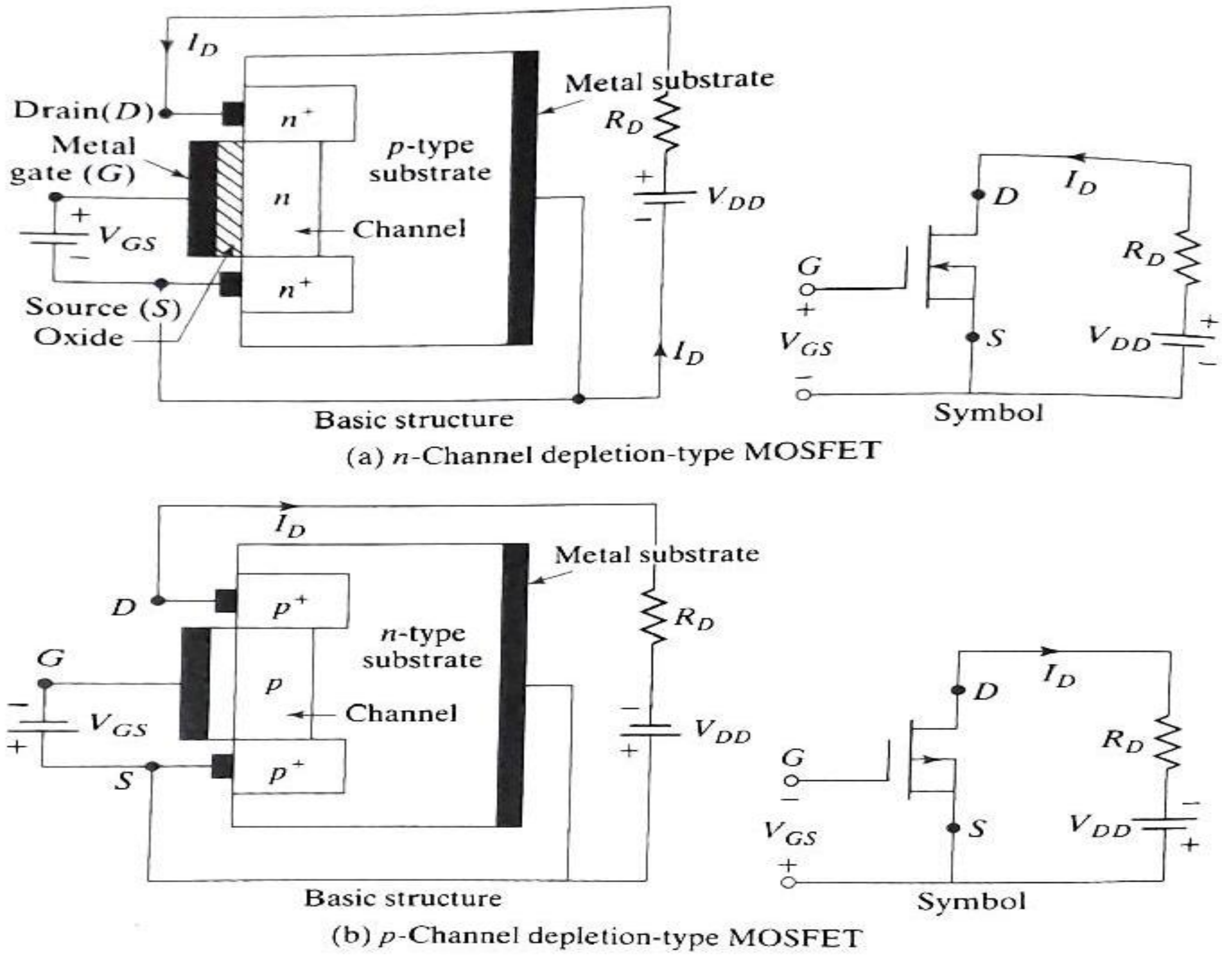

FIGURE 4.1
Depletion-type MOSFETs.

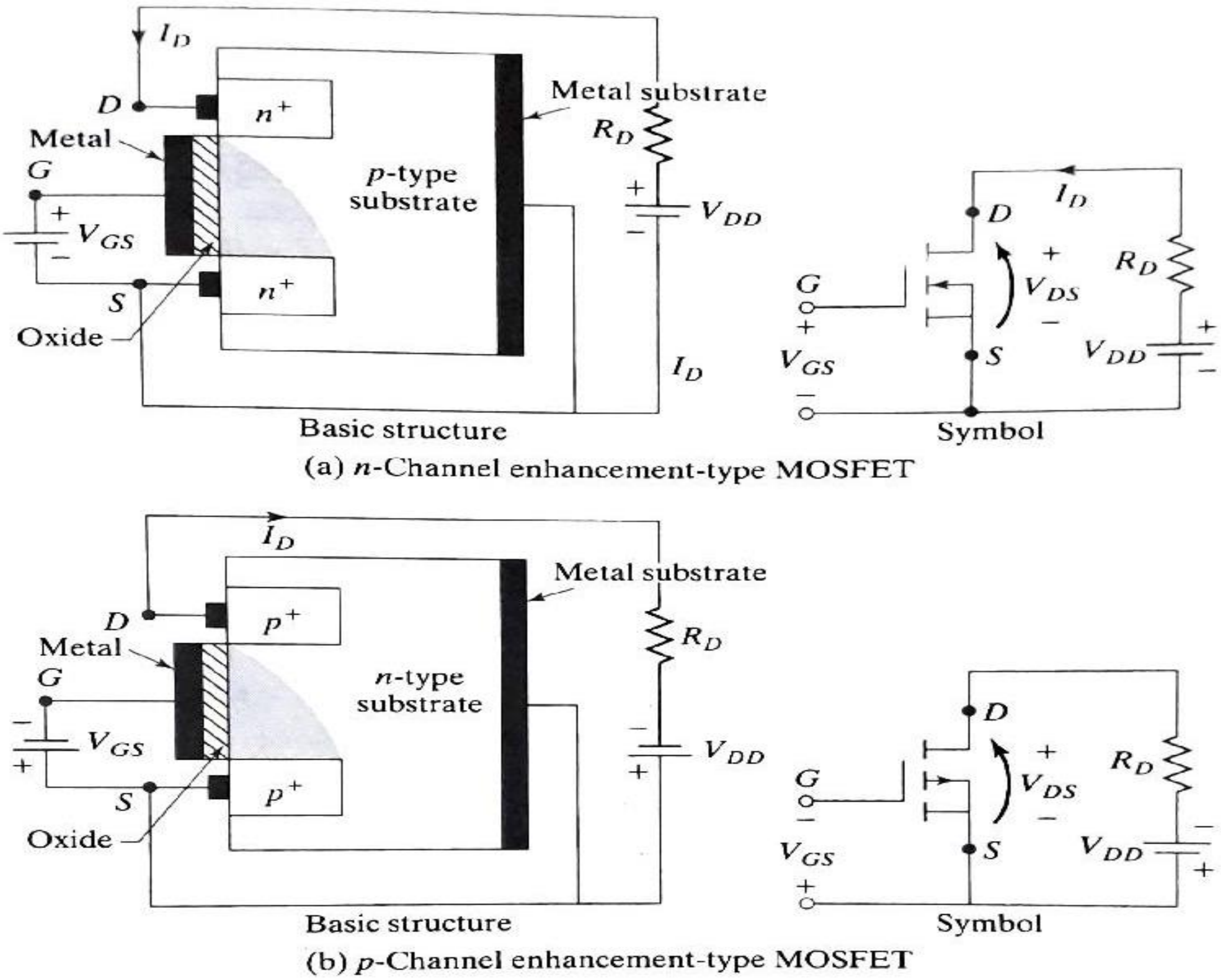

FIGURE 4.2
Enhancement-type MOSFETs.

A few points of differences between the 2 types of MOSFETs along with above Figs.= 5 marks.

NOTE : ***THE QUESTIONS SHOULD BE NEATLY WRITTEN & ANSWERED IN STUDENT'S OWN HANDWRITING. ON TOP OF EACH PAGE, WRITE YOUR NAME & USN BEFORE MAKING A PDF AND UPLOADING THE PDF IN GOOGLE CLASSROOM. TOTAL TIME TAKEN SHOULD NOT EXCEED 2 HOURS FOR BOTH ANSWERING & UPLOADING THE PDF (1.5 HOURS FOR ANSWERING + 0.5 HOURS FOR UPLOADING PDF). PDF SUBMITTED AFTER 2 HOURS OR NOT AS PER THE ABOVE INSTRUCTIONS WILL NOT BE VALUATED AND MARKS ALLOTED WILL BE ZERO FOR THE TEST.***

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