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Internal Assesment Test - I

Sub:	VLSI Design							Code:	18EC72
Date:	11 / 11/ 2021	Duration:	90 mins	Max Marks:	50	Sem:	VII	Branch:	ECE
Answer all the Questions									

		Marks	OBE	
			CO	RBT
1.	Explain the working of an nMOS enhancement mode transistor in different modes of operations with neat diagrams.	[10]	CO1	L1
2.	An nMOS transistor is operated with the following parameters for 90nm technology: V_{GS} =0.9V, V_{th}=0.5V, W=100nm, $\mu_n C_{ox}$ = 90µA/V^2. Find I_{DS} for i) V_{DS} = 0.75V ii) V_{DS} = 1V	[10]	CO1	L2
3.	Explain any two of the following: i) Mobility Degradation ii) Channel length Modulation iii) Body Effect	[5+5]	CO1	L1
4.	Implement the following expression using CMOS logic: i) Y= $\overline{(A+B)(C+D)}$ ii) Y= $\overline{(A + BC)D}$	[5+5]	CO1	L2
5.	Explain the DC transfer characteristics of a CMOS inverter .	[10]	CO1	L1

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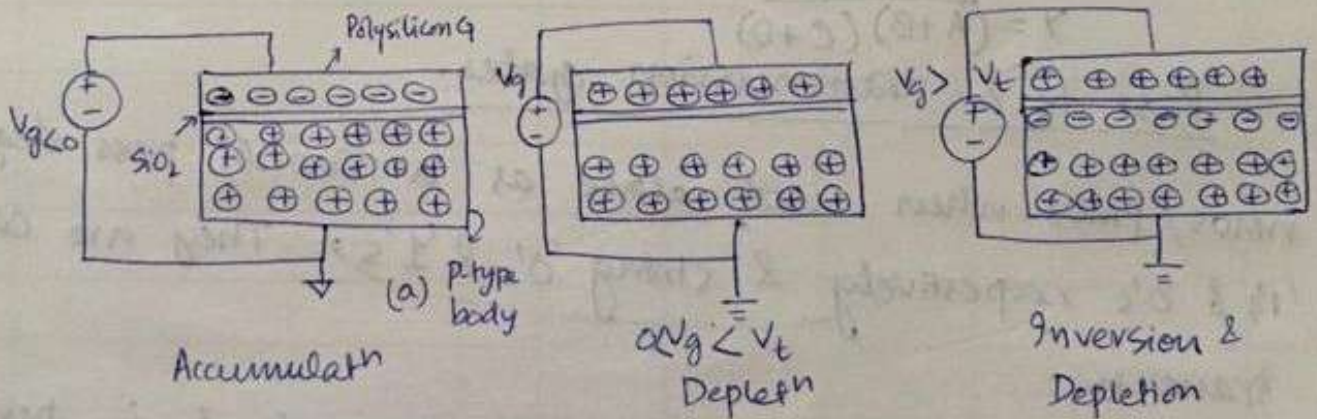
Answer 1

→ The MOS tx is a majority carrier device in which the ct in a conducting channel betn the source & drain is controlled by the gate voltg. In nMOS, $\bar{e}$'s are the majority carriers & in pMOS holes are the majority carriers.

→ Fig shows MOS structure. The top layer is a good conductor called the gate. The middle layer is a very thin insulating film of SiO_2 called gate oxide (about 1000 Å). The bottom layer is doped Si body (p type for n-MOS & n type for PMOS)

→ Op: Let us consider the nMOS type.



In (a), a -ve voltg is applied to the gate, so there is -ve charge on the gate. The mobile +vely charged holes are attracted to the region beneath the gate. This is called accumulatn mode.

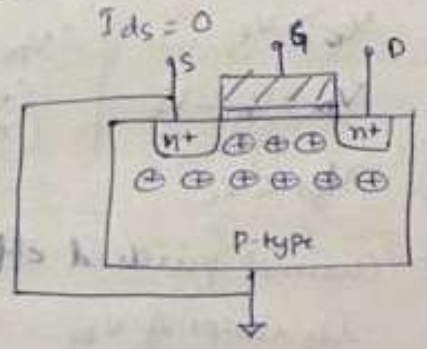
In (b) a small +ve voltg is applied to the gate, resulting

in some +ve charge on the gate. The holes in the body are repelled from the region directly beneath the gate, resulting in ~~some +ve charge~~ a depletion region below the gate.

In(c), a higher +ve voltg exceeding a critical threshold voltg V_t is applied, attracting more +ve charge to the gate. The holes are repelled further and some free $\bar{e}$'s in the body are attracted to the region beneath the gate. This conductive layer of $\bar{e}$'s in the p-type body is called the inversion layer. V_T depends on the no. of dopants in the body and the gate oxide thickness t_{ox}

nMOS op^n

(a) Cut off, no channel



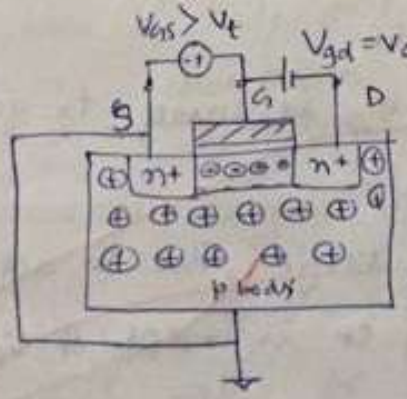
$V_{GS}=0<V_t$

In NMOS, there are 2 n-type regions called source and drain near the gate.

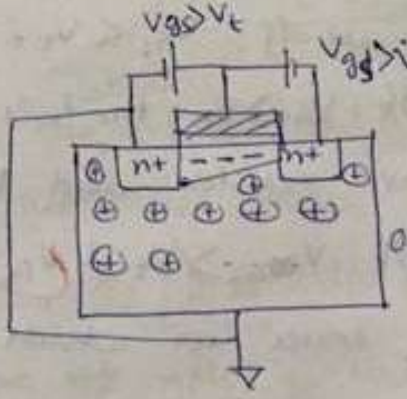
Case 1 Cut off: $I_{ds}=0$, $V_{ds}=0$

$V_{GS}<V_t$: When the gate-to-source voltg V_{GS} is less than V_t, the source & drain have free $\bar{e}$s & the body has free holes. ∴ the source is grounded, the body source & body drain jns are '0' biased or reverse biased, so little or no ct flows and the tx is off. This mode of op^n is called CUTOFF.

Case 2: Linear



$V_{DS}=0$.



$0<V_{ds}<V_{gs}-V_t$.

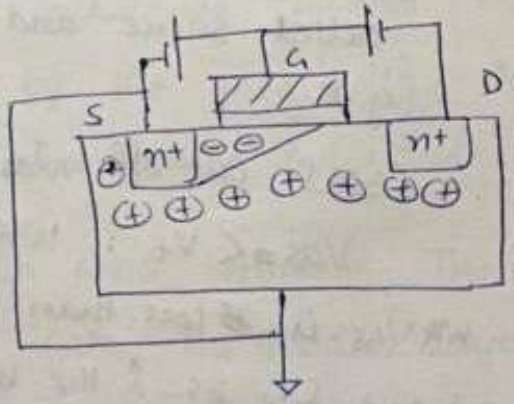
In this region, $V_{GS}>V_t$. As a result an inversion region of $\bar{e}$'s is formed which connects the source & drain creating a conductive path & turning the tx ON. $V_{DS}=V_{GS}-V_{GD}$

Now, if $V_{DS}=0$, $V_{GS}=V_{GD}$ ∴ there is no e.f to push ct

from drain to source. When a small +ve voltg V_{ds} is applied to the drain, ct I_{ds} flows through the channel from ~~source~~ drain to source (ie flow from source → drain). This mode of op^r is called linear, resistive, triode, non-saturated or unsaturated. The ct I_{ds} ↑ with both V_{DS} & V_{GS}.

Case 3: Saturatn.

But if V_{DS} is sufficiently large such that $V_{GD} < V_t$, the channel is no longer inverted near the drain & becomes pinched off. However I_{DS} still flows. ~~under~~ Above the value of V_{DS} when pinch off occurs, I_{ds} is controlled only by the V_{GS} & is no longer influenced by the 'D'. This mode is called saturatn.



$V_{GS} > V_t$

$V_{DS} > V_{GS} - V_t$

$V_{gd} < V_t$.

Channel pinched off.

I_{ds} indpt of V_{DS}

$\Rightarrow V_{GS} > V_t$, $V_{GD} < V_t$

$\therefore V_{DS} = V_{GS} - V_{GD} \Rightarrow V_{DS} > V_{GS} - V_t$

Answer 2

2. Given

$V_{GS} = 0.9V$ $\quad L = 90nm$

$V_{tn} = 0.5\,V$

$W = 100nm$

$\mu_n C_{ox} = 90\mu$

(i) $V_{DS} = 0.75\,V$

(ii) $V_{DS} = 1V.$

$$\beta = \frac{C_{ox} \cdot \mu W}{L} = 90\mu * \frac{100*n}{90*n}$$

$$\boxed{\beta = 100\mu}$$

$V_{gs} > V_t \Rightarrow 0.9 > 0.5$

(i) $V_{gs} - V_t = 0.9 - 0.5 = 0.4 = V_{gt}$

$V_{DS} > V_{gs} - V_t$ — Saturation Region.

$0.75 > 0.4$

Ids @ saturation

$$I_{ds} = \beta \cdot \frac{V_{gt}^2}{2} = \frac{100\mu * (0.4)^2}{2}$$

$$\boxed{I_{ds} = 8\mu A}$$

(ii) $V_{gt} = V_{gs} - V_t = 0.9 - 0.5 = 0.4$.

$V_{ds} > V_{gt}$.

$1 > 0.4$ - True @ saturation.

$$I_{ds} = \frac{\beta \cdot (V_{gt})^2}{2}$$

$$\boxed{I_{ds} = 8\mu A}$$

Answer 3 i)

Mobility degradation :-

- As the vertical field strength increases, the $\left(\frac{V_{gs}}{t_{ox}}\right)$ carriers are scattered in oxide layer of the channel thus slowing the speed / progress.
- As a Result Ids decreases than expected
- the mobility μ is at high Vds.

→ the mobility μ is Replaced by μ_{eff}, which is given by

$$\mu_{eff\text{-}n} = \frac{540 \frac{cm^2}{V.s}}{1 + \left(\frac{V_{gs}+V_t}{0.54 \frac{V}{nm} \cdot t_{ox}}\right)^{1.85}}$$ — μ_{eff} of nmos device

$$\mu_{eff\text{-}p} = \frac{185 \frac{cm^2}{V.s}}{1 + \frac{|V_{gs}+1.5V_t|}{0.388 \frac{V}{nm} \cdot t_{ox}}}$$ - μ_{eff} of pmos device.

At low field strength, Velocity. decreases than Ids also decreases than μ - slop of plot

$$\text{Velocity } v = \begin{cases} \frac{\mu_{eff} \cdot E}{1 + \frac{E}{E_c}} & , E < E_c \\ v_{sat} & , E > E_c \end{cases}$$

@ High electrical field Ec

$$v = v_{dsat}$$

$$v_{dsat} = \frac{\mu_{eff} \cdot E_c}{1 + \frac{E_c}{E_c}}$$

$$v_{dsat} = \frac{\mu_{eff} \cdot E_c}{2}$$

$$\boxed{E_c = \frac{2 v_{dsat}}{\mu_{eff}}} \quad -(2)$$

@ critical voltage $\boxed{V_c = E_c \cdot L}$ -(3).

Then the current Ids is given by using IV characteristic

Ids & Eq (2) & (3)

$$I_{ds} = \begin{cases} \left(\frac{\mu_{eff}}{1 + \frac{V_{ds}}{V_c}}\right) \cdot \frac{C_{ox} \cdot W}{L} \left(V_{gs} - \frac{V_{ds}}{2}\right) V_{ds}, & V_{ds} < V_{dsat} \\ v_{dsat}\, C_{ox} \cdot W \left(V_{gs} - V_{dsat}\right) V_{dsat}, & V_{dsat} < V_{ds} \end{cases}$$

— (4)

The above Equation (4) Represents the Mobility degradation and the μ_{eff} is varied directly on gate source voltage V_{gs}.

3ii)

Channel length Modulation

Onset of saturation mode of opr in MOSFET is signified by pinch-off effect of channel. In saturation, ideally I_{DS} is indpt of V_{DS}. The p-n jn betn the drain & body forms a depletn region and if V_{DS} is increased beyond V_{DSat}, an even larger portn of the channel is pinched off. The effective channel length then reduces to, $L_{eff} = L - L_d$ ——→ (1) where, L_d is the length of the depletn region formed betn body & drain where charge $Q = 0$

With increasing V_{DS}, pinch off pt moves from Drain to source. $\bar{e}$ travelling from S → D traverse the inverted channel length L_{eff} & then they are injected into the depletn region of length L_d that separates the pinch off pt from Drain

Taking Leff into acount, I_{Dsat} can be written as—

$$I_{Dsat} = \frac{\mu C_{ox}}{2} \frac{W}{L^*_{eff}} (V_{GS} - V_t)^2 \longrightarrow (2)$$

$\therefore L^*_{eff} < L$, eqn (2) gives more ct that the ideal ct eqn in satn region under same bias condns.

Rewriting (2) we get

$$I_{Dsat} = \frac{\mu C_{ox} W}{2L} (V_{GT})^2 \left(1 + \frac{V_{ds}}{V_A}\right)$$

where $1 + V_{DS}/V_A$ accounts for channel length modn. $V_A \propto$ channel length & is called early voltg. Channel length modn reduces gain of amplifiers.

3iii) Body effect

Under ideal cond^{n}s, the threshold volt^{g}, V_t is considered const.

But in reality, with increasing ($V_t \uparrow$) source volt^{g}, decreases with the body volt^{g} &, decreases with drain volt^{g} & increases with channel length.

BODY EFFECT

When a voltage V_{SB} is applied betⁿ the source & body, it increases the amt of charge reqd to invert the channel, thereby increasing the threshold volt^{g}, V_t. This effect is called body effect. The threshold volt^{g} is given as -

$$V_t = V_{to} + \gamma\left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}\right) \longrightarrow (1)$$

where, V_{to} is the threshold volt^{g} when source is at body pot.

ϕ_s is the surface pot. at threshold $= 2v_T \ln\frac{N_A}{n_i}$, $\rightarrow (2)$

N_A = doping levels

n_i = intrinsic level of charges

v_T = thermal volt^{g} $= \frac{kT}{q} = 26mV$

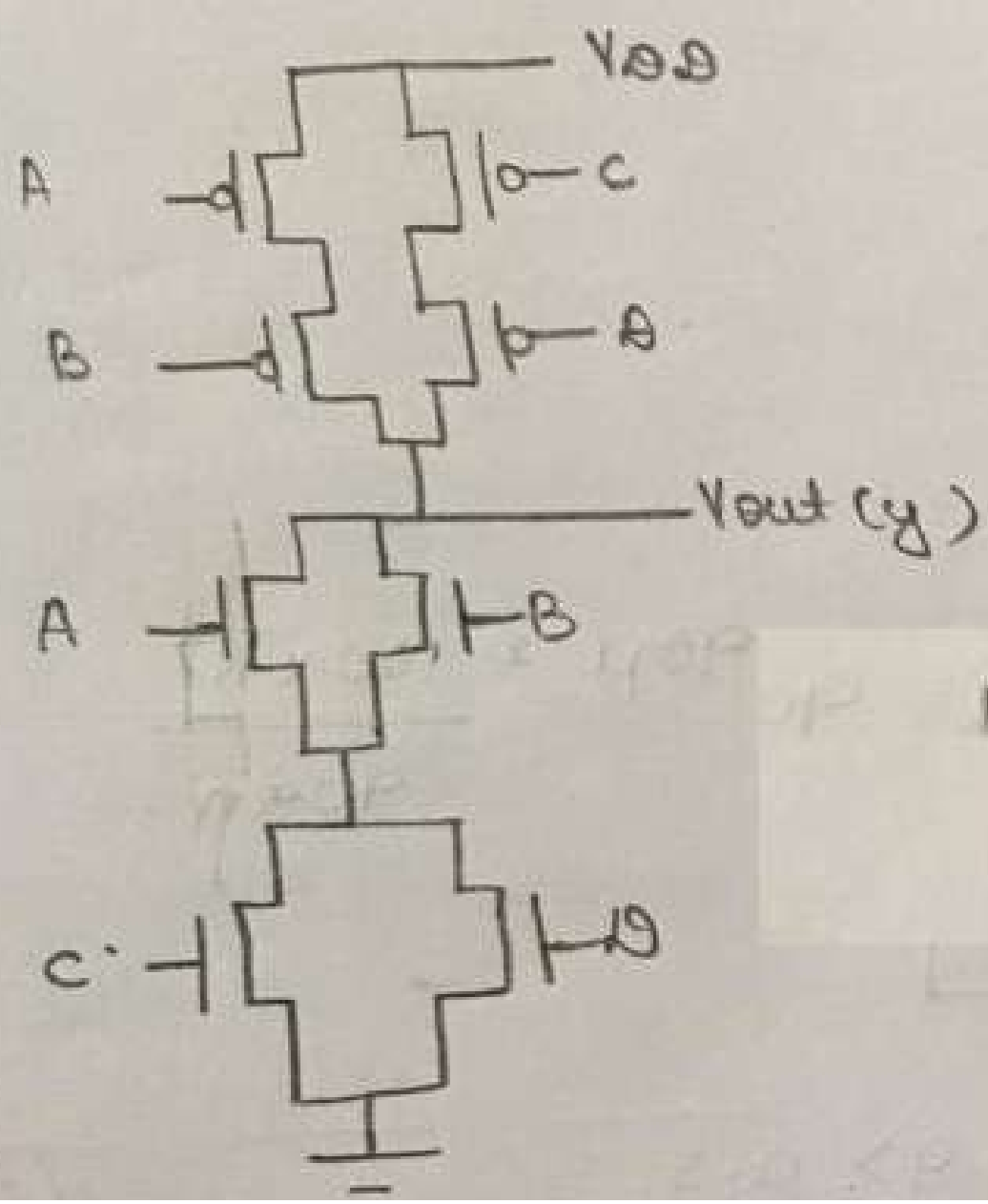
γ = body effect coefficient $\approx$ 0.4 to

$$= \frac{t_{ox}}{\epsilon_{ox}}\sqrt{2q\epsilon_{Si}N_A} = \frac{\sqrt{2q\epsilon_{Si}N_A}}{C_{ox}} \rightarrow (3)$$

$$\epsilon_{Si} = 11.7\epsilon_0$$

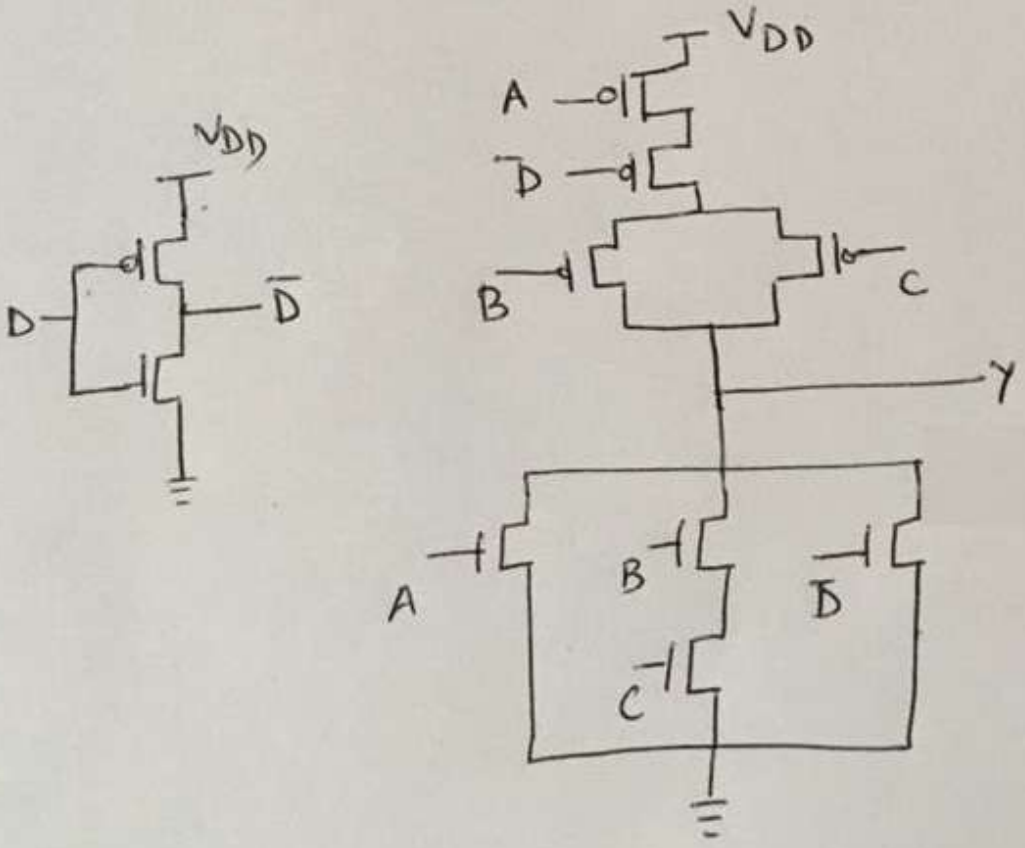
Answer 4

(i) $y = \overline{(A+B)(C+D)}$



Q) 4 ii) $Y = \overline{A + BC}\,D = (\overline{A+BC})(\bar{\bar{D}})$

$= \overline{A + BC + \bar{D}}$ [De Morgan's law]



5 DC Transfer characteristics : DC transfer ch^{r}. of a ckt relate the o/p volts to the I/P volts assuming that the I/P changes slowly enough that capacitances have plenty of time to charge/discharge. A CMOS inverter's DC transfer characteristics can be obtained as follows –

For the CMOS inv. in fig(1)

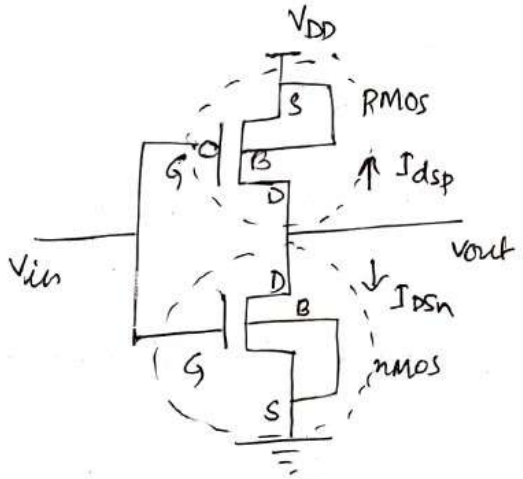


Fig 1 CMOS inv.

Let, V_{GS_n} = gate voltage for nMOS

V_{GSp} = " " " pMOS

$V_{t,n}$ = threshold " " nMOS

$V_{t,p}$ = " " " pMOS.

V_{tn} = +ve volts, V_{tp} = −ve volts

∵ Source of NMOS is grounded, $V_{GSn} = V_{in}$ & $V_{DSn} = V_{out}$

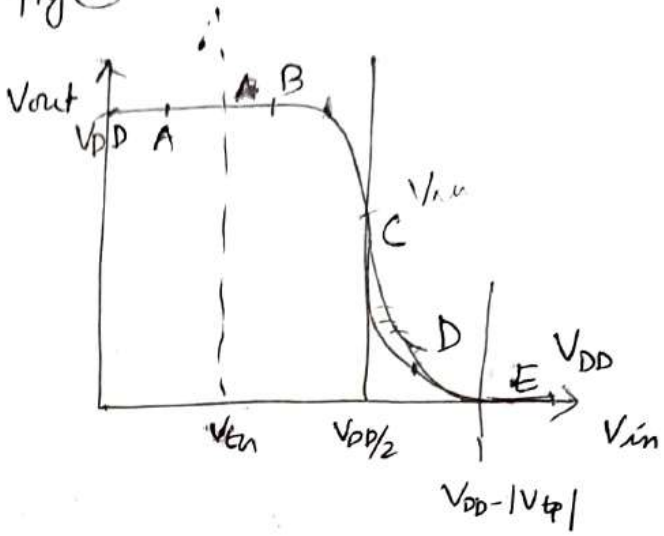
∵ " " pMOS " tied to V_{DD}, $V_{GSp} = V_{in} - V_{DD}$, $V_{DSp} = V_{out} - V_{DD}$

The various regions of op^{r} for the n & p MOS of CMOS are shown in table(1).

	nMOS	PMOS
Cut off:	$V_{GSn} < V_{tn}$ $\therefore V_{in} < V_{tn}$	$V_{GS,p} > V_{tp}$ $V_{in} > V_{tp} + V_{DD}$
Linear	$V_{GSn} > V_{tn}$ $\therefore V_{in} > V_{tn}$. $V_{DS,n} < V_{GSn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{GS,p} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$
Saturation	$V_{GSn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{DSn} > V_{GSn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$	$V_{GSp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

Assuming, $V_{tp} = -V_{tn}$ & $\beta_n = \beta_p$, $I_{dsn} = |I_{DSP}|$

the op^n of CMOS inv. can be classified into 5 regions- as shown in table(2). & fig (2)



1) In reg^n A, nMOS is OFF so pMOS pull o/p to V_{DD}.

2) In region B, nMOS starts to turn ON, pulling the o/p down to '0'.

3) In region C both p & nMOS are in sat^n. (This is the only region present in ideal transistors. for $V_{in} = V_{DD}/2$ & slope is $-\infty$ corresponding to infinite gain. Real tx$_s$. have finite o/p resistances on account of channel length mod^n & thus have finite slopes over a broader region)

4). In region D, pMOS is partially ON & in E it is completely off, leaving nMOS to pull o/p to GND.

Region	Cond^n	pMOS	nMOS	o/p
A	$0 \le V_{in} < V_{tn}$	linear	cut-off	$V_{out} = V_{DD}$
B	$V_{tn} < V_{in} < V_{DD}/2$	"	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	sat.	"	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	"	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	"	$V_{out} = 0$