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Internal Assessment Test 2 – December 2021(Solutions)

Sub:	POWER ELECTRONICS					Sub Code:	17EC73/ 15EC73	Branch:	ECE	
Date:	21-12-2021 (Tuesday)	Duration: (2pm to 3.30pm)	90 mins	Max Marks:	50	Sem/Sec:	7th 'E'			OBE

Answer any FIVE FULL Questions

		MARKS	CO	RBT
1	a)	[10= 3+7]	CO1 & CO2	L3

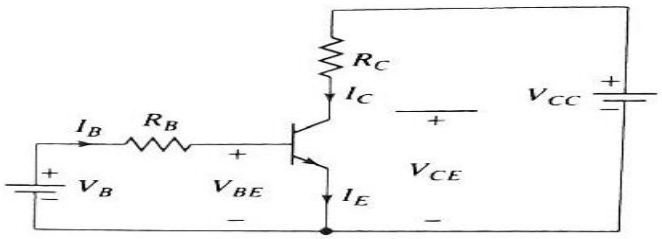


FIGURE 4.31
Transistor switch.

The bipolar transistor in Figure 4.31 is specified to have β_F in the range of 8 to 40. The load resistance is $R_C = 11\ \Omega$. The dc supply voltage is $V_{CC} = 200$ V and the input voltage to the base circuit is $V_B = 10$ V. If $V_{CE(sat)} = 1.0$ V and $V_{BE(sat)} = 1.5$ V, find (a) the value of R_B that results in saturation with an ODF of 5, (b) the β_{forced}, and (c) the power loss P_T in the transistor.

Soln.

$V_{CC} = 200$ V, $\beta_{min} = 8$, $\beta_{max} = 40$, $R_C = 11\ \Omega$, ODF = 5, $V_B = 10$ V, $V_{CE(sat)} = 1.0$ V, and $V_{BE(sat)} = 1.5$ V. From Eq. (4.28), $I_{CS} = (200 - 1.0)/11 = 18.1$ A. From Eq. (4.29), $I_{BS} = 18.1/\beta_{min} = 18.1/8 = 2.2625$ A. Equation (4.30) gives the base current for an overdrive factor of 5,

$$I_B = 5 \times 2.2625 = 11.3125 \text{ A}$$

a. Equation (4.23) gives the required value of R_B,

$$R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.7514\ \Omega$$

b. From Eq. (4.31), $\beta_{forced} = 18.1/11.3125 = 1.6$.

c. Equation (4.32) yields the total power loss as

$$P_T = 1.5 \times 11.3125 + 1.0 \times 18.1 = 16.97 + 18.1 = 35.07 \text{ W}$$

b) Explain two transistor analogy of SCR. Using two transistor analogy, derive expression for anode current in terms of gate current.

Soln.

- The operation of an SCR can be also explained in a very simple way considering it in terms of 2 transistors.
- This is known as the 2 transistor analogy of the SCR.
- The SCR can be considered as an **npn** & a **pnp** transistor, where the collec of one transistor is attached to the base of the other & **vice-versa**, as shc in Fig.1.4.
- The model is obtained by splitting the 2 middle layers of the SCR int separate parts.

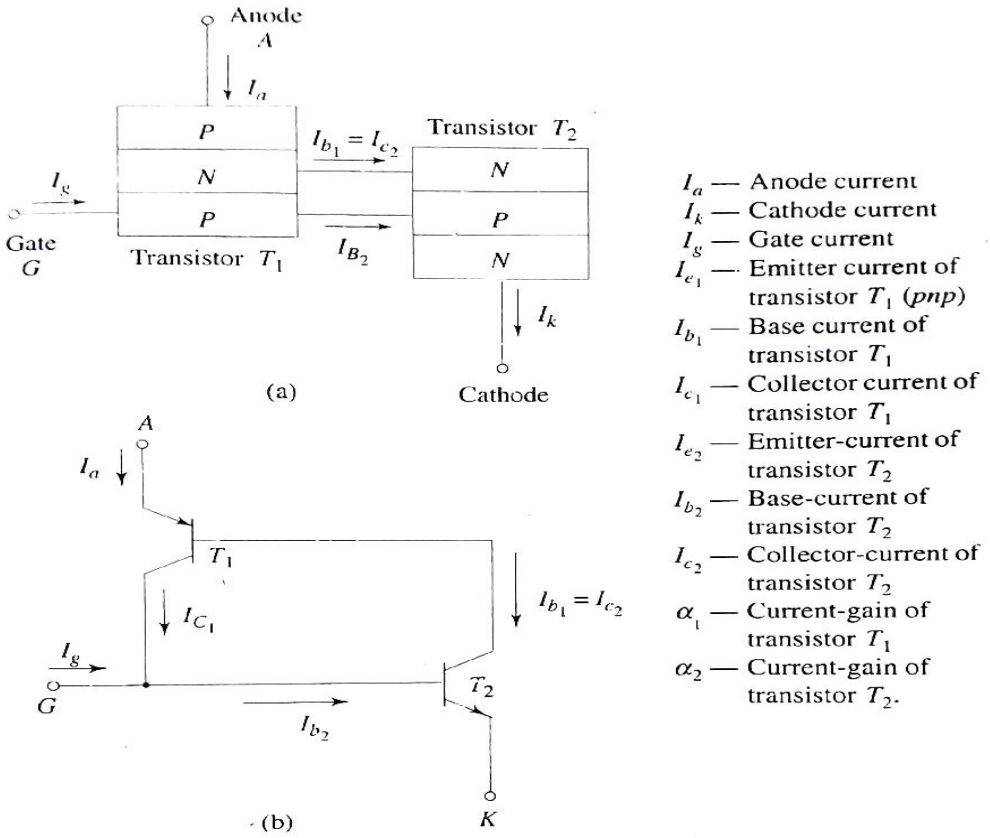


Fig. 1.4 Two transistor analogy of SCR

It is observed from the figure that the collector current of transistor T_1 becomes the base current of transistor T_2 and *vice versa*.

$$\therefore \quad I_{c_1} = I_{b_2} \quad \text{and} \quad I_{b_1} = I_{c_2}$$

Also, $$I_k = I_a + I_g \tag{1.1}$$

Now, we have the relation from transistor analysis,

$$I_{b_1} = I_{e_1} - I_{c_1} \tag{1.2}$$

Also, $$I_{c_1} = \alpha_1 I_{e_1} + I_{co_1} \tag{1.3}$$

where I_{co_1} is the reverse leakage current of the reverse biased junction J_2 when the two outer layers are not present.

Substituting Eq. (1.3) in Eq. (1.2) we get

$$I_{b_1} = I_{e_1} - \alpha_1 I_{e_1} - I_{co_1}.$$

$$I_{b_1} = (1 - \alpha_1) I_{e_1} - I_{co_1}$$

From Fig. 1.4, it is evident that the anode current of the device becomes the emitter current of transistor T_1 that is

$$I_a = I_{e1}$$

$$\therefore \quad I_{b_1} = (1 - \alpha_1) I_a - I_{co_1} \tag{1.4}$$

Also, $$I_{c_2} = \alpha_2 I_{e_2} + I_{co_2}$$

From the Fig. 1.4, it is also observed that the cathode current of the SCR becomes the emitter-current of transistor T_2.

$$\therefore \quad I_k = I_{e_2}$$

$$\therefore \quad I_{c_2} = \alpha_2 I_k + I_{co_2} \tag{1.5}$$

But $$I_{b_1} = I_{c_2} \tag{1.6}$$

Substituting Eqs (1.4 and (1.5) in Eq. (1.6), we get

$$(1 - \alpha_1) I_a - I_{co_1} = \alpha_2 I_k + I_{co_2} \tag{1.7}$$

Substituting Eq. (1.1) in Eq. (1.7), we get

$$(1 - \alpha_1) I_a - I_{co_1} = \alpha_2 (I_a + I_g) + I_{co_2}$$

$$(1 - \alpha_1 - \alpha_2) I_a = \alpha_2 I_g + I_{co_2} + I_{co_1}.$$

$$[1 - (\alpha_1 + \alpha_2)] I_a = \alpha_2 I_g + I_{co_1} + I_{co_2}$$

$$\therefore \quad I_a = \frac{\alpha_2 I_g + I_{co_1} + I_{co_2}}{[1 - (\alpha_1 + \alpha_2)]} \tag{1.8}$$

Assuming the leakage current of transistor T_1 and T_2 to be negligible small, we have

$$I_a = \frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)} \tag{1.9}$$

2 With the help of a suitable circuit and relevant waveforms, explain the following turn-OFF methods of SCR. [10]

i) Natural commutation
ii) Class-A commutation with series load
iii) Class-A commutation with the load in parallel
iv) Class-B commutation

Soln.

- The term **commutation** basically means the transfer of current fr one path to another.
- In thyristor circuits, this term is used to describe process transferring current from one thyristor to another.
- It is not possible for a thyristor to turn itself off.
- The circuit in which it is connected must reduce the thyristor curr to zero to enable it to turn-off.
- 'Commutation' is the term to describe the methods of achieving th

A thyristor can only operate in 2 modes : OFF state (open circuit), or (state (short circuit).

By itself, it cannot control the level of current or voltage in a circuit.

Control can only be achieved by variation in the time when the thyrist are switched ON & OFF.

Commutation is central to this switching process.

There are, in general, two methods by which a thyristor can be commutat

They are :

1.Natural Commutation

2.Forced Commutation

1) Natural Commutation

- The simplest & most widely used method of commutation makes of the alternating, reversing nature of a.c. voltages to effect the curr transfer.

- In a.c. circuits, the current always passes through zero every h cycle.
- As the current passes through natural zero, a reverse voltage v simultaneously appear across the device.
- This immediately turns off the device.
- This process is called as **natural commutation**, since no exter circuit is required for this purpose.
- This method may use a.c. mains supply voltages or the a.c. volta generated by local rotating machines or resonant circuits.
- The line commutated converters and inverters comes under t category.

2) Forced Commutation.

- Once thyristors are operating in the ON state, carrying forw current, they can only be turned OFF by reducing the current flow through them to zero.
- This needs to be done for sufficient time to allow the removal charged carriers.
- In d.c. circuits, for switching off the thyristors, the forward curr should be forced to be zero by some external circuits.
- This process is called **forced commutation** & the external circu required for it are known as commutation circuits.
- The components (inductance & capacitance) which constitute commutating circuits are called as commutating components.
- A reverse voltage is developed across the device by means o commutating circuit.
- This circuit immediately brings the forward current in the device zero, thus turning off the device.
- Producing reliable commutation is a difficult problem to be tack while designing chopper & inverter circuits.

- The most important stage in the designing process is choosing a for turn-off method & deciding its components.
- The classification of the methods of forced commutation is based
  - ✓ The arrangement of the commutating components.
  - ✓ The manner in which zero current is obtained in the SCR.
- There are 6 basic methods of commutation by which thyristors n be turned OFF.
- 2 of these methods will be dealt with in detail as follows.

Class A-self commutation by resonating the load :

This is also known as resonant commutation.

This type of commutation circuit using L-C components-in-series-with load are shown in Fig.1.12.

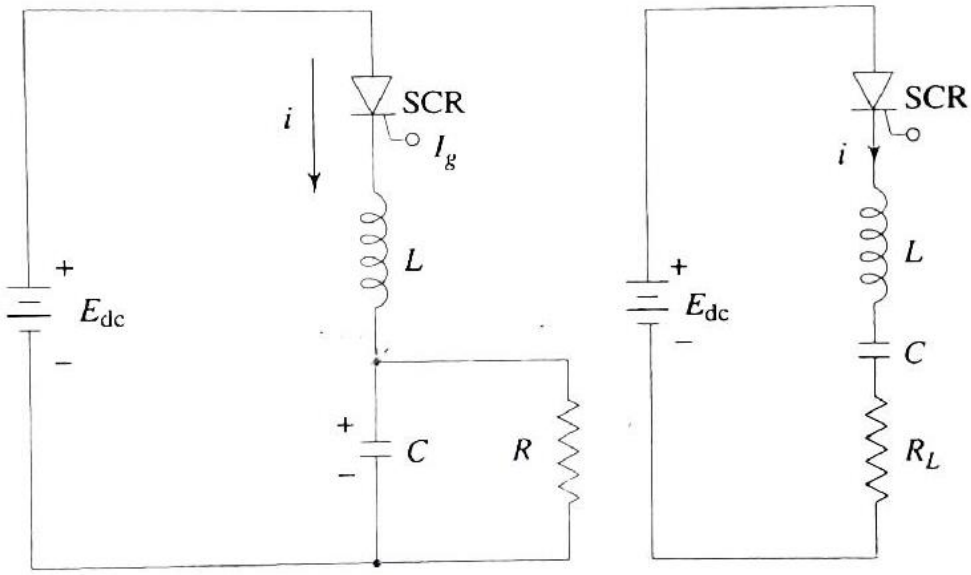
In Fig.1.12(a), load RL is in parallel with the capacitor & in Fig.1.12(load RL is in series with the L-C circuit.

In this process of commutation, the forward current passing through device is reduced.

It is reduced to less than the level of holding current of the device.

Hence, this method is also known as the current commutation method.

The waveforms of the thyristor voltage, current & capacitor voltages shown in Fig.1.13.



(a) Load in parallel with capacitor

(b) Load in series with capacitor

Fig. 1.12 Class A commutation circuit

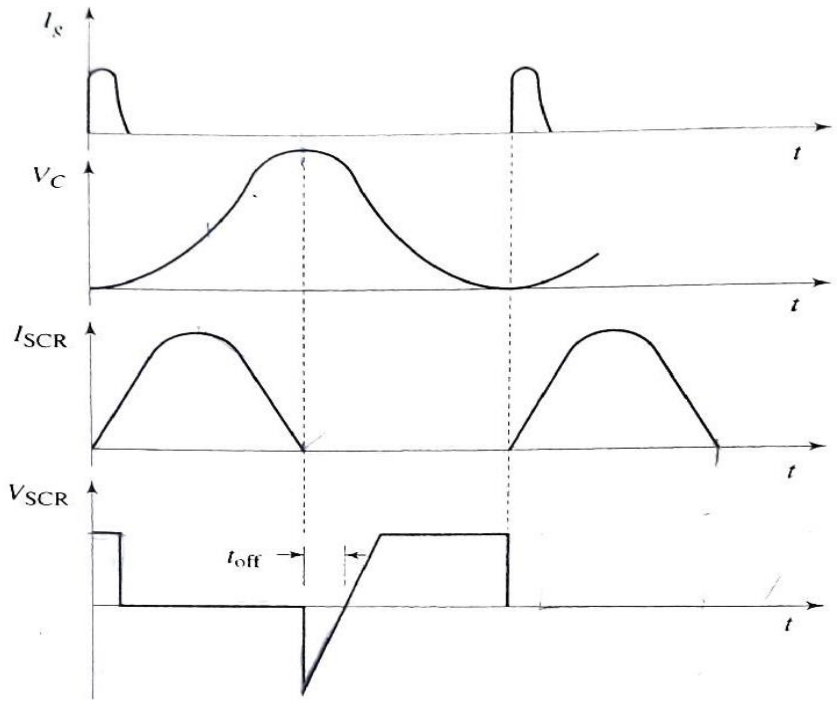
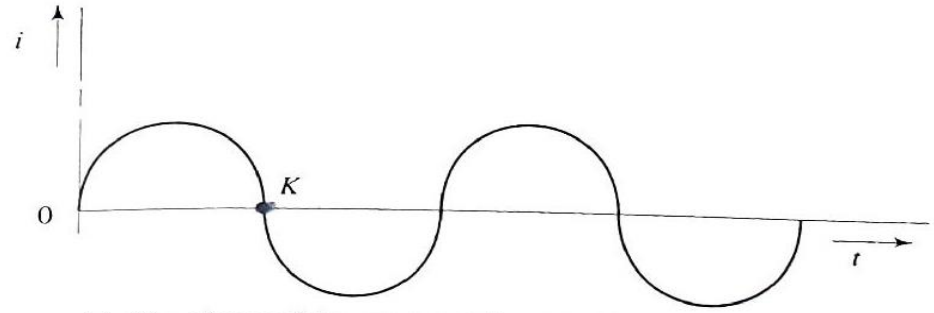
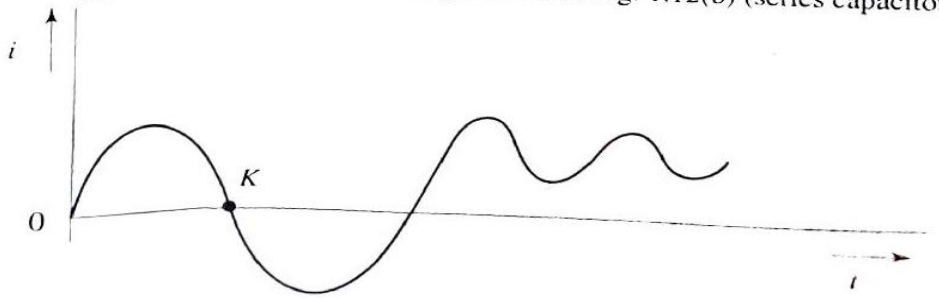


Fig. 1.13 Voltages and currents in Class A (load is parallel with capacitor)



(a) Waveforms of the current produced in Fig. 1.12(b) (series capacitor)



(b) Waveforms of the current produced in Fig. 1.12(a) (parallel capacitor)

Fig. 1.14

Class B-self commutation by an LC circuit:

- In this method, the LC resonating circuit is across the SCR & not series with the load.
- The commutating circuit is shown in Fig.1.15 & the associa waveforms are shown in Fig.1.16.
- Initially, as soon as the supply voltage E_{dc} is applied, the capacito starts getting charged.
- It charges upto the voltage E_{dc} , with its upper plate positive & lower plate negative.

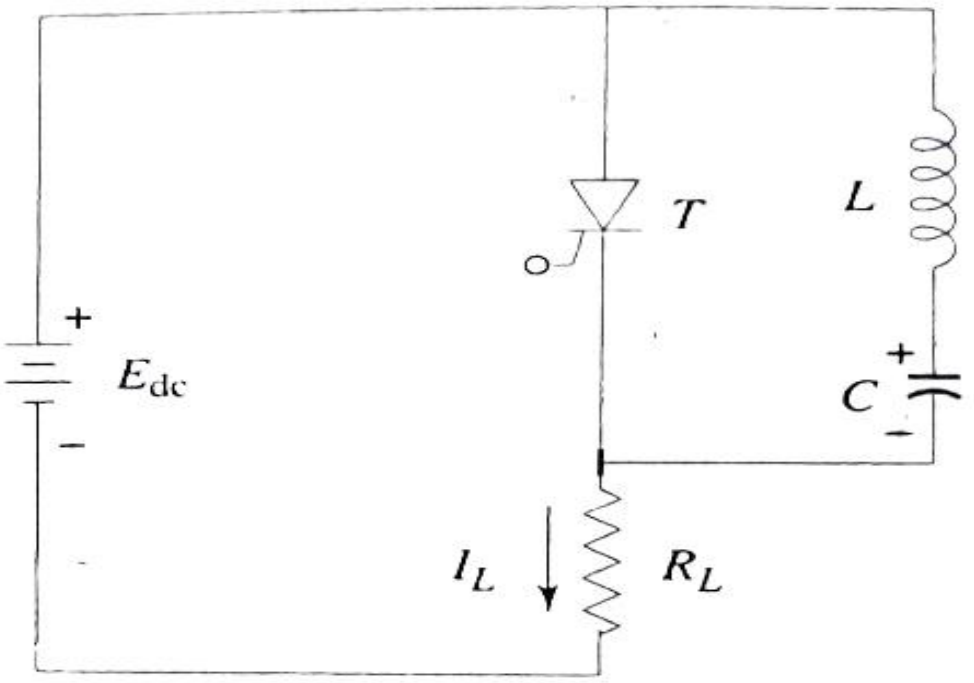


Fig. 1.15 Class B commutation circuit

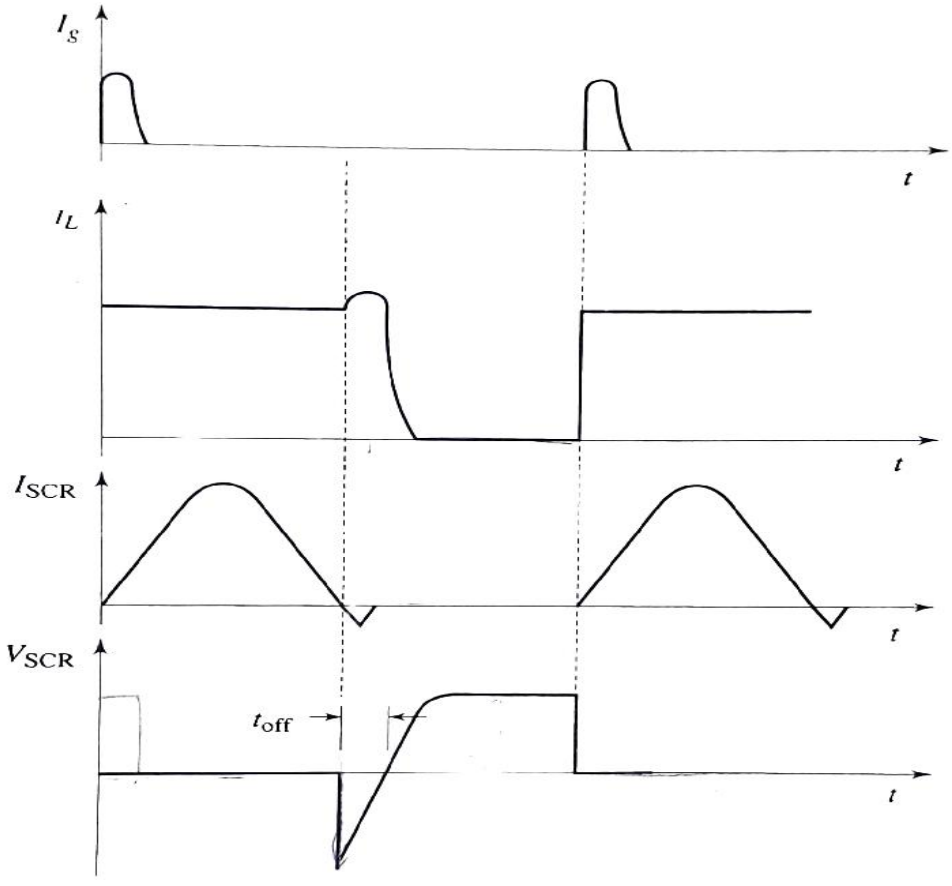


Fig. 1.16 Associated waveforms

3	a) Mention and explain different thyristor turn-on methods. Mention the advantages of gate triggering. **Solution:**	[10= 6+4]	CO2	L2

- A thyristor can be switched from a non-conducting state to a conducting state in several ways as described below.

1.9.1 – Forward Voltage Triggering

- When anode-to-cathode forward voltage is increased with gate circuit open, the reverse biased junction J_2 will have an avalanche breakdown.
- This occurs at a voltage called forward, breakover voltage V_{BO}.
- At this voltage, a thyristor changes from OFF state (high voltage with low leakage current) to ON-state characterised by a low voltage across it with large forward current.
- The forward voltage drop across the SCR during the ON state is of the order of 1 to 1.5V & increases slightly with load current.

1.9.2 – Thermal Triggering (Temperature Triggering)

- Like any other semiconductor, the width of the depletion layer of a thyristor decreases on increasing the junction temperature.
- Thus, in a thyristor, when the voltage applied between anode & cathode is very near to its breakdown voltage, the device can be triggered by increasing its junction temperature.
- When the temp. is increased within specified limits, a situation comes when the reverse bias junction collapses making the device conduct.
- This method of triggering the device by heating is known as the thermal triggering process.

1.9.3 – Radiation Triggering (Light Triggering)

- In this method, as the name suggests, the energy is imparted by radiation.
- Thyristor is bombarded by energy particles such as neutrons or photons.
- With the help of this external energy, electron-hole pairs are generated in the device.
- This increases the number of charge carriers.
- This leads to instantaneous flow of current within the device & the triggering of the device.
- For radiation triggering to occur, the device must have high value of rate of change of voltage (dv/dt).
- Examples : Light activated silicon controlled rectifier (LASCR) & Light activated silicon controlled switch (LASCS).

1.9.4 – dv/dt Triggering

- We know that with forward voltage across the anode & cathode of a device, the junctions J_1 and J_3 are forward biased.
- Junction J_2 becomes reverse biased.
- This reverse biased junction J2 has the characteristics of a capacitor.
- This is due to the charges existing across the junction.
- If a forward voltage is suddenly applied, a charging current will flow tending to turn the device ON.
- If the voltage impressed across the device is denoted by V, the charge by Q and the capacitance by C_j, then,

$$i_c = \frac{dQ}{dt} = \frac{d}{dt}(C_j V) = C_j \frac{dV}{dt} + V\frac{dc_j}{dt} \quad ($$

The rate of change of junction capacitance may be negligible as the jun capacitance is almost constant. The contribution to charging current by the term is negligible. Hence, Eq. (1.13) reduces to

$$i_c = C_j \frac{dV}{dt} \quad (1$$

Therefore, if the rate of change of voltage across the device is large, the d may turn-on even though the voltage appearing across the device is small.

1.9.5 – Gate Triggering

- This is the most commonly used method for triggering SCRs.
- In Laboratories, almost all the SCR devices are triggered by this process.
- By applying a positive signal at the gate terminal of the device, it can be triggered much before the specified breakover voltage.
- The conduction period of the SCR can be controlled by varying the gate signal within the specified values of max. & min. gate currents.
- For gate triggering, a signal is applied between the gate & the cathode of the device.

- 3 types of signals can be used for this purpose.
- They are either d.c. signals, pulse signals or a.c. signals.

1. **D.C. gate triggering**

- ✓ A d.c. voltage of proper magnitude & polarity is applied between the gate & the cathode of the device.
- ✓ This is done in such a way that the gate becomes positive with respect to the cathode.
- ✓ When the applied voltage is sufficient to produce the required gate current, the device starts conducting.
- ✓ Drawback is both power & control circuits are d.c. & there is no isolation between the two.
- ✓ Another disadvantage is that a continuous d.c. signal has to be applied, at the gate causing more gate power loss.

2. A.C. gate triggering

- ✓ A.C. source is commonly used for the gate signal in all application of thyristor control adopted for a.c. applications.
- ✓ This scheme provides the proper isolation between the power & the control circuits.

- ✓ However, the gate drive is maintained for one half cycle after the device is turned ON.
- ✓ Also, a reverse voltage is applied between the gate & the cathode during the negative half cycle.
- ✓ Drawback is that a separate transformer is required to step down the a.c. supply, which adds to the cost.

3. Pulse gate triggering

- ✓ This is the most popular method for triggering the device.
- ✓ In this method, the gate drive consists of a single pulse appearing periodically or a sequence of high frequency pulses.
- ✓ This is known as carrier frequency gating.
- ✓ A pulse transformer is used for isolation.
- ✓ The main advantage of this method is that there is no need of applying continuous signals.
- ✓ Hence, the gate losses are very much reduced.
- ✓ Electrical isolation is also provided between the main device supply & its gating signals.

b) Draw and explain UJT Firing Circuit.

Solution :

- The basic circuit is shown in Fig.2.22.
- The B_1 pulse output is used to trigger the SCR, a predetermined time after the switch is closed.
- Thus, the 1^{st} B_1 pulse occurs T seconds after the 28 V is supplied to the UJT circuit.
- After the SCR has been triggered "on", subsequent pulses at its gate have no effect.
- An important design consideration in this type of circuit concerns the premature triggering of the SCR.
- The voltage at B_1 when the UJT is "off", must be smaller than the voltage needed to trigger the SCR.
- Otherwise, the SCR will be triggered immediately upon switch closure.
- Thus, we have the requirement as follows:

$V_{B_1}(\text{off}) < (I_g \times 1\ \text{k}\Omega + V_g)$

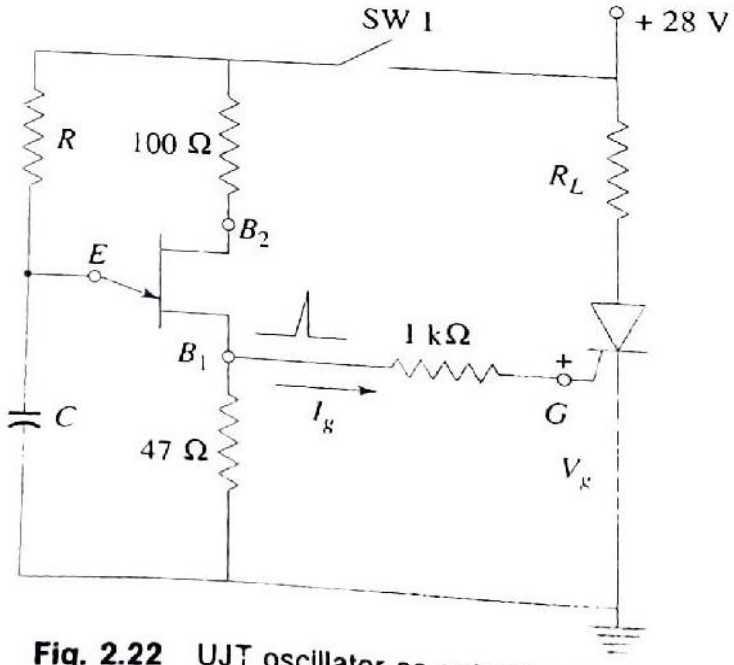


Fig. 2.22 UJT oscillator as gate trigger source

4	a) With a neat figure, explain the static anode-cathode characteristics of a SCR. **Solution :**	[10 = 5+5]	CO2	L2

- An elementary circuit diagram for obtaining static V-I characteristics of a thyristor is shown in Fig.1.2.
- Here, the anode & cathode are connected to the main source through a load.
- The gate & cathode are fed from another source E_g.
- The static V-I characteristic of an SCR is shown in Fig.1.3.
- Here, V_a is the anode-cathode voltage & I_a is the anode current.
- The thyristor V-I characteristic is divided into 3 regions of operation - **Reverse Blocking Region**, **Forward Blocking Region** & **Forward Conduction Region**.

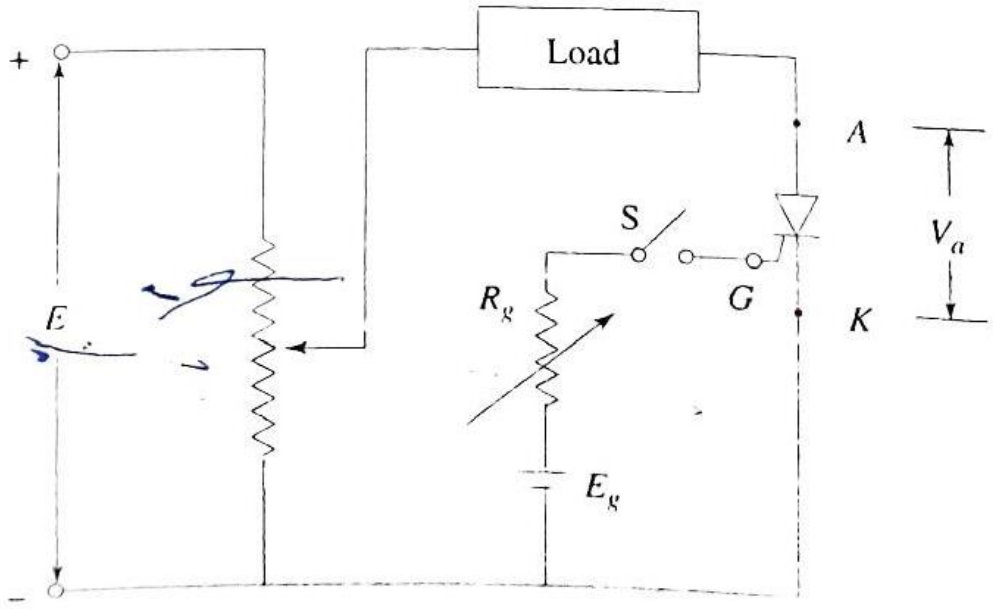
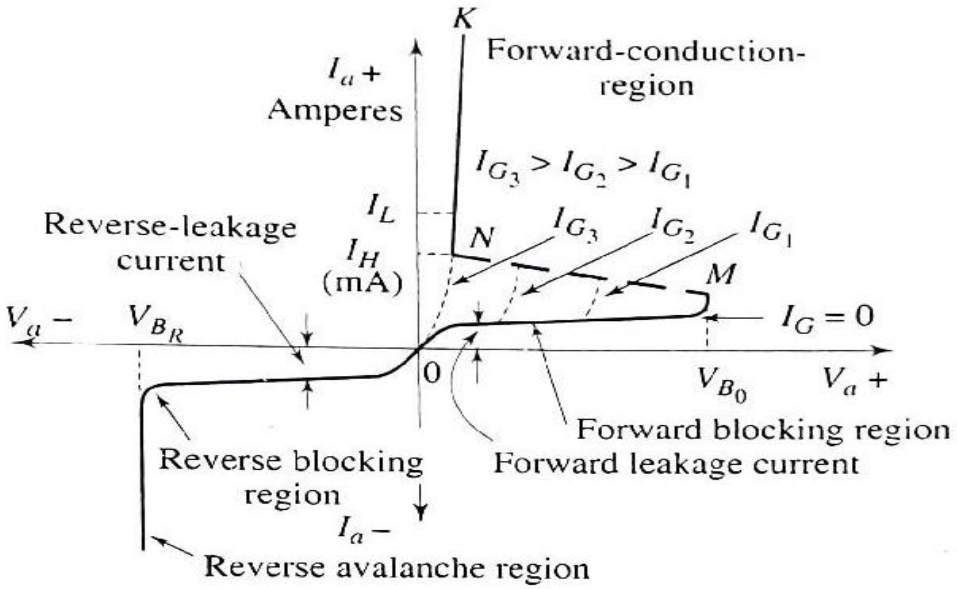


Fig. 1.2 Elementary circuit



V_{B_0} = Forward breakover voltage

V_{B_R} = Reverse breakover voltage

I_G = Gate current

I_L = Latching current

I_H = Holding current

Fig. 1.3 *V-I* characteristics

- These 3 regions of operation are described below.

1. **Reverse Blocking Region :**

- When the cathode is made positive wrt. anode with the switch **s** open (Fig.1.2), the thyristor becomes reverse biased.
- In Fig.1.3, **OP** is the reverse blocking region.
- In this region, the thyristor exhibits a blocking characteristic similar to that of a diode.

- In this reverse biased condition, the outer junctions J_1 & J_3 are reverse biased & the middle junction J_2 is forward biased.
- Hence, only a small leakage current (in mA) flows.
- If reverse voltage is increased, then at a critical breakdown level called **Reverse Breakdown Voltage V_{BR}**, an avalanche will occur at J_1 & J_3 increasing the current sharply.
- If this current is not limited to a safe value, power dissipation will increase to a dangerous level that may destroy the device.
- Region **PQ** is the reverse-avalanche region.
- If reverse voltage is below critical value, the device behaves as a high-impedance device (i.e. essentially open) in the reverse direction.
- The inner 2 regions of the SCR are lightly doped compared to the outer layers.
- The **forward break-over voltage V_{BO}** is generally higher than the **reverse break-over voltage V_{BR}**.
- This is because of thickness of J_2 depletion layer (during forward biased condition) will be greater than the total thickness of the 2 depletion layers at J_1 & J_3 (when the device is reverse biased).

2. Forward Blocking Region :

- In this region, the anode is made positive wrt. the cathode.
- Hence, junctions J_1 & J_3 are forward biased while the junction J_2 remains reverse biased.
- Therefore, the anode current is a small forward leakage current.
- The region **OM** of the V-I characteristic is known as the **forward blocking region** when the device does not conduct.

3. Forward Conduction Region :

- When the anode to cathode forward voltage is increased with the gate circuit kept open, avalanche breakdown occurs.
- This occurs at the junction J_2 at a critical forward break-over voltage (**V_{BO}**).
- The SCR then switches into a low impedance condition (high conduction mode).
- In Fig.1.3, the forward breakover voltage is corresponding to the point **M**, when the device latches on to the conducting state.

- The region **MN** of the characteristic shows that as soon as the device latches on to its **on** state, the voltage across the device drops, from say, several hundred volts to 1-2 volt.
- This results in a very large amount of current suddenly flowing through the device.
- The part NK of the characteristic is called as the forward conduction state.
- In this high conduction mode, the external load impedance is essentially determines the anode current (Thyristor can be regarded as a closed switch).

- Once the SCR is conducting a forward current that is greater than the minimum value, called the **latching current**, the gate signal is not required to maintain the device in its on state.
- Removal of the gate current does not affect the conduction of the anode current.
- The SCR will return to its original forward blocking state if the anode current falls below a low level, called the **holding current (I_h).**
- Latching current is associated with the turn-on process & holding current with the turn-off process.
- The holding current is usually lower than, but very close to the latching current.

b) With neat circuit diagram and waveforms, explain RC - Half wave firing circuit.

Solution :

- Figure 2.12 shows the RC-half wave trigger circuit.
- By the RC network, a larger variation in the value of the firing angle can be obtained.
- This is by changing the phase & amplitude of the gate current.
- By varying the resistor R_v, the firing angle can be controlled from 0 to 180^o.
- In the negative half cycle, capacitor C charges through diode D_2 with lower plate positive to the peak supply voltage E_{max}.
- This capacitor voltage remains constant at $-E_{max}$ until supply voltage attains zero value.

- Now, as the SCR anode voltage passes through zero & becomes positive, capacitor C begins to charge through R_v from the initial voltage $-E_{max}$.

- When the capacitor charges to positive voltage equal to gate trigger voltage V_{gt} (= $V_{g(min)}$ +V_{D1}), SCR is triggered.
- After this, the capacitor holds to a small positive voltage, as shown in Fig.2.12.
- During negative half cycle, the diode D_1 prevents the breakdown of the gate to cathode junction.
- In the range of power-frequencies, the RC for zero output voltage is given by

$$R_v C \geq \frac{1.3T}{2} = \frac{4}{w} \tag{2.4}$$

where $T = 1/f$ = period of ac line frequency in seconds.

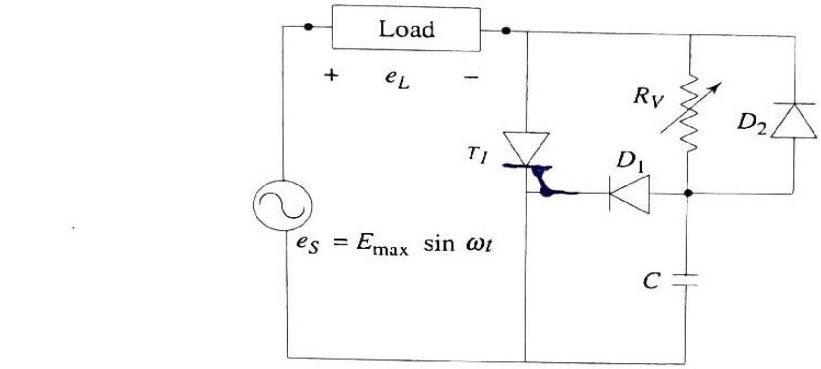
As discussed above, the thyristor will turn on when the capacitor voltage e_c equals $(V_{g(min)} + V_{D1})$, provided the gate current $I_{g(min)}$ is available. Therefore, the maximum value of R_v is given by

$$\begin{aligned} e_s &\geq I_{g(min)} R_v + e_c \\ &= I_{g(min)} R_v + V_{g(min)} + V_{D1} \end{aligned} \tag{2.5}$$

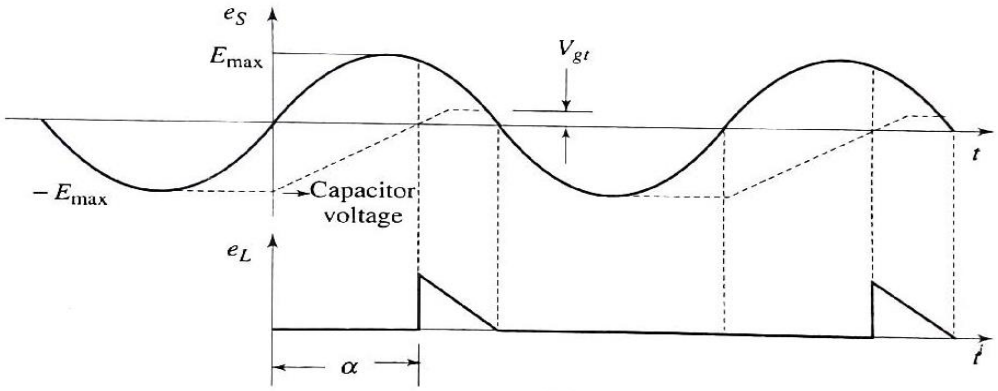
or

$$R_v \leq \frac{e_s - V_{g(min)} - V_{D1}}{I_{g(min)}} \tag{2.6}$$

where e_s is the instantaneous supply voltage at which the thyristor will turn on. From Eqs 2.4 and 2.6, the suitable values of R_v and C can be obtained.



(a)



(b)

Fig. 2.12 (a) RC firing circuit, (b) voltage-waveform

5	a) Explain with Structure & symbol, the principle of operation of SCR. **Solution:** • The structure & symbol of the thyristor (SCR) are shown in Fig.1.1. • It is a 4 layered PNPN switching device, having 3 junctions J_1, J_2 and J_3. • It has 3 external terminals, namely, the anode (A), cathode (K) and gate (G). • The anode & cathode are connected to the main power circuit. • The gate terminal carries a low level gate current in the direction of gate to ca • Normally, the gate terminal is provided at the P layer near the cathode. • This is known as cathode gate.	[10= 05+05]	CO2	L2

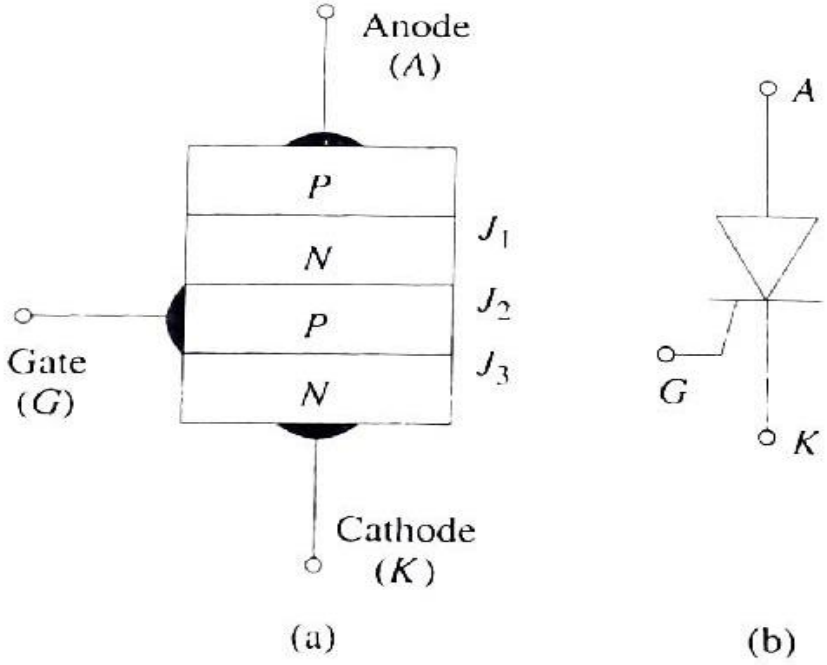


Fig. 1.1 (a) Structure (b) symbol

- When the end P layer is made positive with respect to the end N layer, the junctions, J_1 & J_3 are forward biased.
- But, the middle junction J_2 becomes reverse biased.
- The junction J_2, due to depletion layer, does not allow any current to flow thrc device.
- Leakage current, negligibly small in magnitude, flows through the device du drift of the mobile charges.
- This current is insufficient to make the device conduct.
- The depletion layer, mostly of immobile charges do not constitute any flow of
- Thus, the SCR does not conduct under forward biased condition.
- This is called as the **forward blocking state** or off state of the device.

- When the end n layer is made positive with respect to the end p layer, the junction J_2 becomes forward biased.
- The other 2 junctions, J_1 and J_3 become reverse biased.
- The junctions J_1 & J_3 do not allow any current to flow through the device.
- Only a very small amount of leakage current may flow because of the drif charges.
- The leakage current is again insufficient to make the device conduct.
- This is known as the **reverse blocking state** or off state of the device.

- The width of the depletion layer at the junction J_2 decreases with the increase i to cathode voltage.
- This is because the width is inversely proportional to voltage.
- If the voltage between anode & cathode is increased beyond a value (called **f break-over voltage**), the depletion layer at J_2 vanishes.
- The reverse biased junction J_2 will breakdown due to the large voltage gradien its depletion layer.
- This phenomenon is known as the **Avalanche Breakdown**.

- As the other 2 junctions, J_1 & J_3 are already forward biased, there will be a free movement across all the 3 junctions.
- This results in a large amount of current flowing through the device from a cathode.
- Due to the flow of this forward current, the device starts conducting & it is th to be in the **conducting state** or on state.

b) With neat circuit diagram and waveforms, explain Resistance firing circuit.

Solution :

- The circuit in Fig.2.11 shows a simple method for varying the trigger a therefore, the power in the load.
- Instead of using a gate pulse to trigger the SCR, the gate current is supplied by source of voltage e_s.
- This is done through R_{min}, R_v, and the series diode D.
- The circuit operates as follows :

(i) As e_s goes positive, the SCR becomes forward-biased from anode to cathode; however, it will not conduct ($e_L = 0$) until its gate current exceeds $I_{g(min)}$.

(ii) The positive e_s also forward biases the diode and the SCRs gate–cathode junction; this causes flow of a gate current i_g.

(iii) The gate current will increase as e_s increases towards its peak value. When i_g reaches a value equal to $I_{g(min)}$, the SCR turns "on" and e_L will approximately equal e_s (refer to point P on the waveform in Fig. 2.11).

(iv) The SCR remains "on" and $e_L \approx e_s$ until e_s decreases to the point where the load current is below the SCR holding-current. This usually occurs very close to the point until $e_s = 0$ and begins to go negative.

(v) The SCR now turns "off" and remains "off" while e_s goes negative since its anode–cathode is reverse biased, and since the SCR is now an open switch, the load voltage is zero during this period.

(vi) The purpose of the diode in the gate-circuit is to prevent the gate–cathode reverse bias from exceeding peak reverse gate voltage during the negative half-cycle of e_s. The diode is chosen to have peak reverse-voltage rating greater than the input voltage E_{max}.

(vii) The same sequence is repeated when e_s again goes positive.

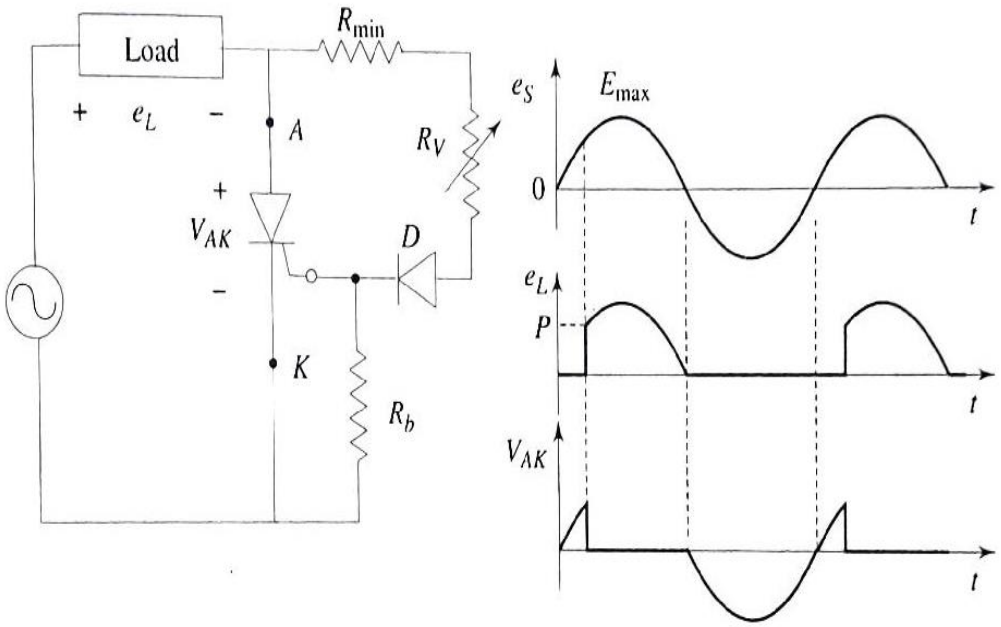


Fig. 2.11 R-firing circuit and associated voltage waveforms

- The load-voltage waveform in Fig.2.11 can be controlled by varying R_v whic the resistance in the gate circuit.
- If R_v is increased, the gate current will reach its trigger value $I_{g(min)}$ at a great of e_s.
- This makes the SCR to trigger at a latter point in the e_s positive half-cycle.
- Thus, the trigger angle α will increase.
- The opposite will occur if R_v is decreased.
- If R_v is made large enough, the SCR gate current will never reach $I_{g(min)}$ & t will remain "off".
- The minimum trigger angle is obtained with R_v equal to zero.

- As shown in Fig.2.11, the limiting resistor $R_{(min)}$ is placed between anode and
- It is placed in such a way that the peak gate current of the thyristor I_{gm} is not ex
- When the supply voltage has reached its peak, E_{max} ,

$$R_{min} \geq \frac{E_{max}}{I_{gm}} \qquad (2.1)$$

- The stabilizing resistor R_b should have such a value that the max. voltage dro it does not exceed max. possible gate voltage $V_{g(max)}$.
- From the voltage distribution,

$$R_b \leq \frac{(R_v + R_{min}) \cdot V_{g(max)}}{(E_{max} - V_{g(max)})} \qquad (2.2)$$

The thyristor will trigger when the instantaneous anode voltage, e_s , is

$$e_s = I_{g(min)} (R_v + R_{min}) + V_d + V_{g(min)} \qquad (2.3)$$

where $I_{g(min)}$ = minimum gate current to trigger the thyristor
V_d = voltage drop across the diode
$V_{g(min)}$ = gate-voltage to trigger, corresponding to $I_{g(min)}$.

6 With a circuit diagram and waveform, explain the working of a single-phase full converter with RL load. Derive an expression for the average and rms voltage across the load. [10] CO3 L2

Solution :

- The circuit arrangement of a single-phase full converter is shown in Figure10.1a with a highly inductive load.
- This enables load current to be continuous and ripple free.
- During the positive half cycle, thyristors T_1 & T_2 are forward biased.
- When these 2 thyristors are turned on simultaneously at $\omega t = \alpha$, the load is connected to the input supply through T_1 & T_2.
- Due to the inductive load, thyristors T_1 & T_2 continue to conduct beyond $\omega t = \pi$, even though the input voltage is already negative.

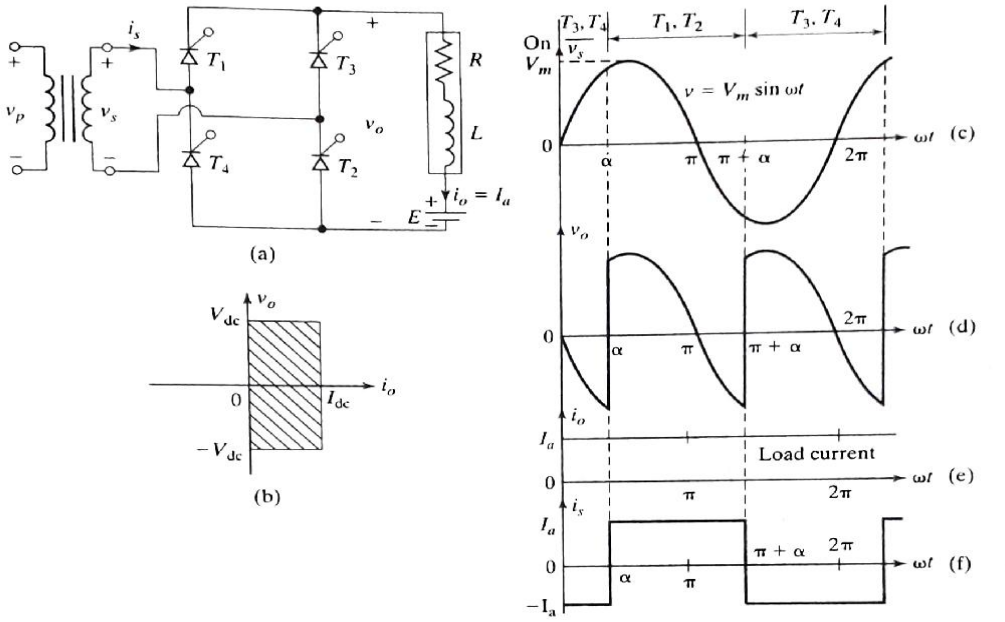


FIGURE 10.1

Single-phase full converter. (a) Circuit, (b) Quadrant, (c) Input supply voltage, (d) Output voltage, (e) Constant load current, and (f) Input supply current.

- During the negative half-cycle of the input voltage, thyristors T_3 & T_4 are forward biased.
- The turning on of thyristors T_3 & T_4 applies the supply voltage across thyristors T_1 & T_2 as reverse blocking voltage.
- T_1 & T_2 are turned off due to **line or natural commutation** & the load current is transferred from T_1 & T_2 to T_3 & T_4.
- Figure 10.1b shows the regions of converter operation.
- Figures 10.1c-f show the waveforms for input voltage, output voltage, & input and output currents.

- During the period from α to π, the input voltage v_s & input current i_s are positive, & power flows from the supply to the load.
- The converter is said to be operated in **rectification** mode.
- During the period from π to π + α, the input voltage v_s is negative & the input current i_s is positive.
- Hence, reverse power flows from the load to the supply.
- The converter is said to be operated in **inversion mode**.
- This converter is extensively used in industrial applications up to 15 kW.
- Depending on the value of α, the average output voltage could be either positive or negative, & it provides 2-quadrant operation.

The average output voltage can be found from

$$V_{dc} = \frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin \omega t \, d(\omega t) = \frac{2V_m}{2\pi}[-\cos \omega t]_{\alpha}^{\pi+\alpha}$$

$$= \frac{2V_m}{\pi}\cos \alpha \qquad (10.1)$$

and V_{dc} can be varied from $2V_m/\pi$ to $-2V_m/\pi$ by varying α from 0 to π. The maximum average output voltage is $V_{dm} = 2V_m/\pi$ and the normalized average output voltage is

$$V_n = \frac{V_{dc}}{V_{dm}} = \cos \alpha \qquad (10.2)$$

The rms value of the output voltage is given by

$$V_{rms} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2} = \left[\frac{V_m^2}{2\pi}\int_{\alpha}^{\pi+\alpha} (1 - \cos 2\omega t) \, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2}} = V_s \qquad (10.3)$$

With a purely resistive load, thyristors T_1 and T_2 can conduct from α to π, and thyristors T_3 and T_4 can conduct from $\alpha + \pi$ to 2π.

7 What is a dual converter? Explain its operation with a neat circuit diagram. [10] CO3 L2

Solution :

- Single-phase full converters with inductive loads allow only a two-quadrant operation.
- 2 of these full converters are connected back to back, as shown in Figure 10.2a.
- This enables both the output voltage and the load current flow to be reversed.
- Thus, the system provides a 4-quadrant operation & is called a **dual converter**.
- Dual converters are normally used in high-power variable-speed drives.

- If α_1 and α_2 are the delay angles of converters 1 and 2, respectively, the corresponding average output voltages are V_{dc1} and V_{dc2}.
- The delay angles are controlled.
- This is done such that one converter operates as a rectifier & the other converter operates as an inverter.
- But, both converters produce the same average output voltage.
- Figures 10.2b-f show the output waveforms for 2 converters, where the 2 average output voltages are the same.

- Figure 10.2b shows the V-I characteristics of a dual converter.

From Eq. (10.1) the average output voltages are

$$V_{dc1} = \frac{2V_m}{\pi}\cos\alpha_1 \tag{10.11}$$

and

$$V_{dc2} = \frac{2V_m}{\pi}\cos\alpha_2 \tag{10.12}$$

Because one converter is rectifying and the other one is inverting,

$$V_{dc1} = -V_{dc2} \quad \text{or} \quad \cos\alpha_2 = -\cos\alpha_1 = \cos(\pi - \alpha_1)$$

Therefore,

$$\alpha_2 = \pi - \alpha_1 \tag{10.13}$$

Because the instantaneous output voltages of the two converters are out of phase, there can be an instantaneous voltage difference and this can result in circulating current between the two converters. This circulating current cannot flow through the load and is normally limited by a *circulating current reactor* L_r, as shown in Figure 10.2a.

If v_{o1} and v_{o2} are the instantaneous output voltages of converters 1 and 2, respectively, the circulating current can be found by integrating the instantaneous voltage difference starting from $\omega t = \pi - \alpha_1$. Because the two average output voltages during the interval $\omega t = \pi + \alpha_1$ to $2\pi - \alpha_1$ are equal and oppositive, their contributions to the instantaneous circulating current i_r is zero.

$$\begin{aligned} i_r &= \frac{1}{\omega L_r}\int_{\pi-\alpha_1}^{\omega t} v_r\, d(\omega t) = \frac{1}{\omega L_r}\int_{\pi-\alpha_1}^{\omega t} (v_{o1} + v_{o2})\, d(\omega t) \\ &= \frac{V_m}{\omega L_r}\left[\int_{2\pi-\alpha_1}^{\omega t} \sin\omega t\, d(\omega t) - \int_{2\pi-\alpha_1}^{\omega t} -\sin\omega t\, d(\omega t)\right] \\ &= \frac{2V_m}{\omega L_r}(\cos\alpha_1 - \cos\omega t) \quad i_r > 0 \quad \text{for} \quad 0 \le \alpha_1 < \frac{\pi}{2} \\ &\qquad\qquad i_r < 0 \quad \text{for} \quad \frac{\pi}{2} < \alpha_1 \le \pi \end{aligned} \tag{10.14}$$

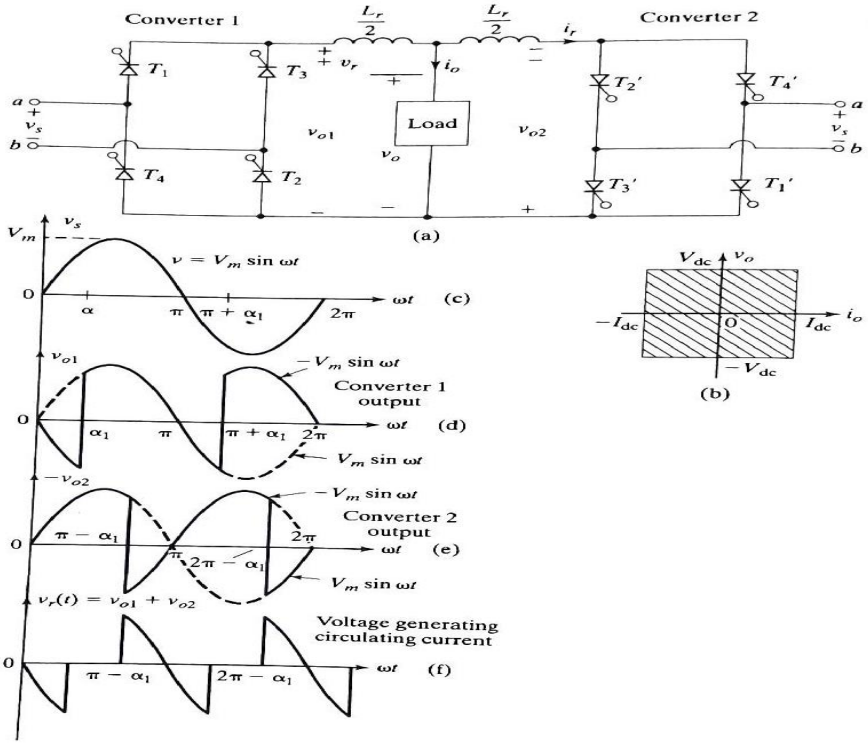


FIGURE 10.2
Single-phase dual converter. (a) Circuit, (b) Quadrant, (c) Input supply voltage, (d) Output voltage for converter 1, (e) Output voltage for converter 2, and (f) Circulating inductor voltage.

8	a) What is a thyristor? How does it differ from a diode and transistor? **Solution :** Thyristor is a 3 terminal device (Anode, Cathode, Gate) having 4 PN layers and 3 PN junctions. It is an important semiconductor device in power electronics. A diode has only 1 pn junction and no gate terminal as compared to thyristor. A transistor has 2 pn junctions and its terminals are Emitter, Base & Collector. b) What is forced commutation? How does it differ from natural commutation? **Solution :** When the input signal is DC across anode to cathode, the thyristor cannot be turned off without the use of external circuitry to forcefully reduce the current to zero and apply reverse bias voltage from anode to cathode. This is called forced commutation. It differs from natural commutation in that in natural commutation, the input signal is ac in nature and hence naturally reduces itself to zero and goes negative. This process then turns off the thyristor without a need for external circuitry. c) With neat graph, explain gate characteristics of a SCR. **Solution :** • In a thyristor, the gate is connected to the cathode through a PN junction & resembles a diode.	[10 = 3+3+4]	CO2	L2

- Therefore, the V-I characteristic of a gate is similar to a diode but varies considerably in units.
- The circuit that supplies firing signals to the gate must be designed:

1) To accommodate these variations.
2) Not to exceed the maximum voltage, & power capabilities of the gate.
3) To prevent triggering from false signals or noise.
4) To assure desired triggering.

- **Figure 1.7 shows the gate characteristics of a typical SCR.**
- **Here, positive gate to cathode voltage V_g & positive gate to cathode current I_g represent d.c. values.**
- **Applying gate drive increases the minority carrier density in the inner P layer.**
- **This facilitates the reverse breakdown of the junction J_2.**
- **There are max. & min. limits for gate voltage & gate current.**
- **This prevents the permanent destruction of junction J3 & provides reliable triggering.**
- **There is also a max. limit on instantaneous gate power-dissipation ($P_{gmax} = V_g * I_g$), which depends on the type of gate drive.**
- **The gate signal can be d.c. or a.c. or a sequence of high frequency pulses.**
- **With pulse firing, a larger amount of Pg can be tolerated if the average-value of Pg is within permissible limits & hence gate can be driven harder using pulse firing.**
- **This provides for reliable & faster turn-on of the device.**
- **All possible safe operating points for the gate are bounded by the low & high current limits for the V-I characteristics, max.gate voltage, & the hyperbola representing max. gate power.**

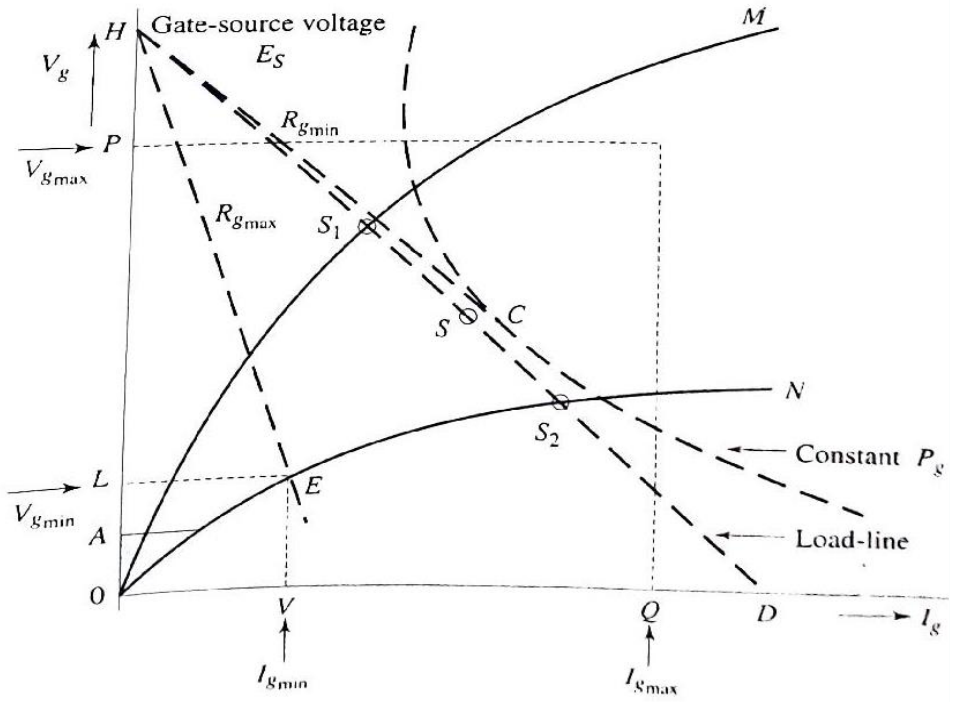


Fig. 1.7 Gate characteristics

- Within these boundaries there are 3 regions of importance.

1) The 1st region OA lies near the origin.

- It is defined by the max.gate voltage that will not trigger any device.
- This region sets a limit on the max. false signals that can be tolerated in the gate firing circuit.

2) The 2nd region is defined by the min.value of gate-voltage & current required to trigger all devices at the min.rated junction temperature.

- It is a forbidden region for the firing circuit as a signal in this region may not always fire all devices or never fire any at all.
- In Fig.1.7, OL & OV are the min. gate voltage & gate current limits respectively.

3) The 3rd region is the largest & shows the limits on gate-signal for reliable firing.

- In Fig.1.7, curves ON & OM correspond to the possible spread of the characteristic for SCRs of the same rating.
- For best results, the operating point S , which may change from S_1 to S_2, must be as close as possible to the permissible P_g curve.
- S must also be contained within the max. & min. limits of gate voltage & gate current.
- This provides the necessary hard drive for the device.

- For selecting the operating point, usually a load line of the gate source voltage E_s=OH is drawn as HD.
- The gradient of the load line HD(=OH/OD) will give the required gate source resistance R_g.
- The max. value of this series resistance is given by the line HE.
- E is the point of intersection of lines indicating the min.gate voltage & gate current.
- The min. value of gate source series resistance is obtained by drawing a line HC tangential to P_g curve.
- A thyristor may be considered to be a charged controlled device.
- Higher the magnitude of the gate current pulse, lesser is the time needed to inject the required charge for turning on the thyristor.
- The SCR turn-on time can be reduced by using gate current of higher magnitude.
- Pulse width should be sufficient to allow anode current to exceed the latching current.
- In practice, gate pulse width T $\geq$ ton (SCR turn-on time) (Fig.1.8 shows T).

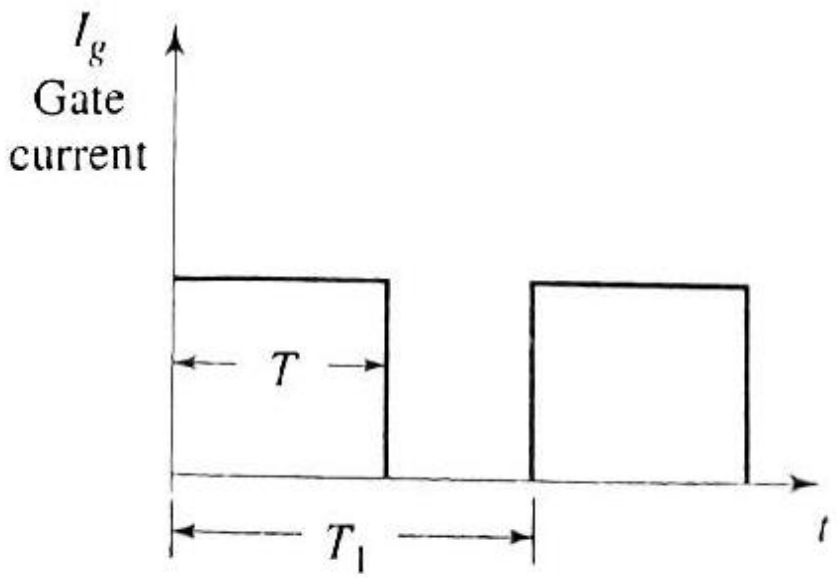


Fig. 1.8 Pulse gating

$$T \geq t_{on}$$

With pulse firing, if the frequency of firing f is known, the peak instantaneou gate power dissipation $P_{g_{max}}$ can be obtained as

$$P_{g_{max}} = V_g I_g = \frac{P_{g_{av}}}{f T} \quad (1.10)$$

where $f = \frac{1}{T_1}$ = frequency of firing or pulse repetition rate in Hz

and T = pulse width in second

A duty cycle is defined as the ratio of pulse on period to the periodic time c pulse. In the Fig. 1.8 pulse-on period is T and the periodic time is T_1. Therefor duty-cycle is given by

$$\delta = \frac{T}{T_1} = fT \quad (1.11$$

From Eq. (1.10)

$$\frac{P_{g_{av}}}{\delta} \leq P_{g_{max}} \quad (1.12$$

ALL THE BEST