Case-3: then $S=1, R=1 \Rightarrow \bar{S}=0, \bar{R}=0$

When $\bar{S}=0$ $Q=1$ &

$Q=1$; $\bar{R}=0 \Rightarrow \bar{Q}=1$

∴ Contradiction is taking place, the o/p $\bar{Q}$ should be complementary of Q.

Taking $\bar{S}=1, \bar{R}=1$

from NAND gate-1; $\bar{S}=1$, $Q=1$

$Q=1, \bar{R}=1 \Rightarrow \bar{Q}=0$

from this; $S=1, R=1$

$Q=0, \bar{Q}=1$

since it is retaining the previous o/p [Contradiction is taking place].

Case-4: When $\bar{S}=0$, $\bar{R}=0$ forbidden state.

Truth Table of $\bar{S}\bar{R}$ latch:-

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	Forbidden state (not used)	
0	1	1	0 (Set state)
1	0	0	1 (Reset state)
1	1	previous o/p (Memory)	

3) Ring Counter:- It is a circular shift register in which the value will not lost if it is retained in a circular manner.

Mod-6 Ring counter logic diagram:-

→ Let the initial state is "1000"

→ Assuming all the flip-flops are in positive edge triggered counting sequence:-

clk	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1
↓	1	0	0	0

→ Getting back the initial state.

→ Ring counter are used in decode counter.

5) D flip flop :

Truth Table :-

clk	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

characteristic table which predicts the next state

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

∴ characteristic Equation is;

$Q_{n+1} = D$

Excitation table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T flip flop :-

Truth Table :-

clk	T	Q_{n+1}
0	X	Q_n (No change)
1	0	Q_n
1	1	$\bar{Q}_n$ (Toggle)

characteristic table :-

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

∴ characteristic Equation is;-

$Q_{n+1} = \bar{Q}_n T + \bar{T} Q_n \Rightarrow Q_{n+1} = Q_n \oplus T$

Excitation table :-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

→ Let the initial bit "1011"
→ Assuming all the flipflops are positive edge triggered

clk	Q_0	Q_1	Q_2	Q_3
↓	1	1	0	1
↓	1	1	1	0
↓	0	1	1	1
↓	1	0	1	1
↓	1	1	0	1

→ Serial Data out.

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for K_1 :

Q_1 \ Q_2Q_3	00	01	11	10
0	X	X	X	X
1		1	X	X

$K_1 = Q_3$

for J_2 :

Q_1 \ Q_2Q_3	00	01	11	10
0		1	X	X
1			X	X

$J_2 = \overline{Q_1}Q_3$

for K_2 :

Q_1 \ Q_2Q_3	00	01	11	10
0	X	X	1	
1	X	X	X	X

$K_2 = Q_3$

for J_3 :

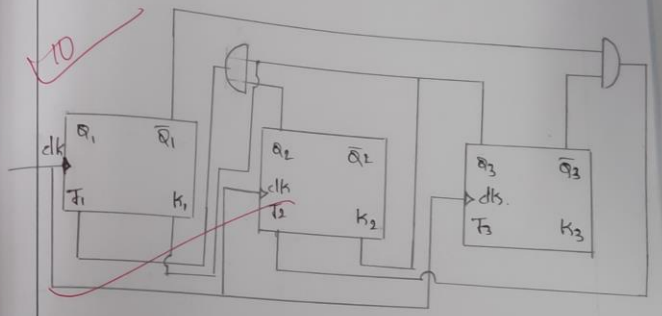
Q_1 \ Q_2Q_3	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$J_3 =$

for K_3 :

Q_1 \ Q_2Q_3	00	01	11	10
0	X	1	1	X
1	X	1	X	X

Circuit diagram:-



Johnson Counter:- It is also called as Twisted ring Counter (or) Switch tail Counter

→ Mod-8 Johnson Counter / Mod-8 ring Counter

Logic diagram

→ let the initial state is "0000"

→ Assuming all flipflops are positive edge triggered counting sequence;

clk	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

→ Getting back the initial state

→ Totally are used 8 decade counters.

4) PISO :- Unidirectional parallel in serial out.

→ Data is (B_3-B_0) fed through B_3 to B_0.

→ We have two modes in this case;

load → data is fed parallely inside

shift → data is shifted one from flip

serially out

→ shift/load is active low - '0', therefore load is '1' in this case load will fed the data parallel -ly inside from B_3 to B_0

→ shift/load is active high - '1', therefore shift is '1' in this shift will fed the data inside serially from B_3 to B_0

→ B_3 - MSB, & B_0 is LSB

6) MOD 6 synchronous up counter:-

∴ No of states is 6

∴ No of flipflops used is 3 FFs

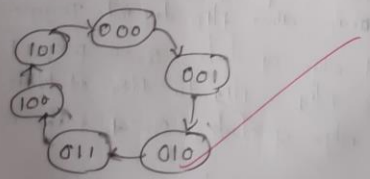
Let the sequence be:

Q_1	Q_2	Q_3	
0	0	0	(0)
0	0	1	(1)
0	1	0	(2)
0	1	1	(3)
1	0	0	(4)
1	0	1	(5)

∴ (6, 7) ⇒ don't care

0 0 0

→ state diagram:-



Excitation table for JK flip flop:-

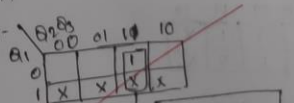
Q^t	Q^{t+}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table for counter:-

present state			next state			FFs input			
Q_1^t	Q_2^t	Q_3^t	Q_1^{t+}	Q_2^{t+}	Q_3^{t+}	J_1 K_1		J_2 K_2		J_3	K_3
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

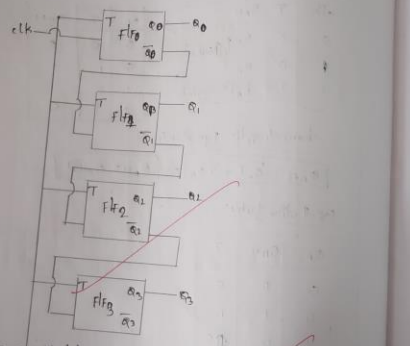
K-Map:-

for J_1 :-



$J_1 = Q_2 Q_3$

4- bit ripple counter



Count enable = 1

→ Let the initial state is "0000"

→ Assuming all the flipflops are positive edge triggered

Counting sequences:

clk	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
↓	0	0	0	1
↓	0	0	1	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	0	1
↓	0	1	1	0
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	0	1
↓	1	0	1	0
↓	1	0	1	1
↓	1	1	0	0
↓	1	1	0	1
↓	1	1	1	0
↓	1	1	1	1

L 10 very good!!

→ Ripple counter has a counting sequence.

→ During 1st positive edge of clock, $Q_0 = 1$, & the FF_0 is affected, whereas other FFs don't get Toggle.

→ During second edge of clock, $Q_0 = 0$ & $\overline{Q}_0 = 1$ it is input at a clock to FF_1 ∴ FF_1 to FF_3 will Toggle.

→ During third edge of clock, $Q_0 = 1$ & $\overline{Q}_0 = 0$, then FF_0 is toggled.

→ During fourth edge of clock, $Q_0 = 0$ & $\overline{Q}_0 = 1$, it is input at a clock to FF_1 ∴ FF_2 to FF_3 it will Toggle.