## **COA IAT3 Scheme and Solution Feb 2022**

1. Explain single bus organization of datapath in a processor with a neat diagram. (10)

Diagram-5 M

Explanation on each block-5 M

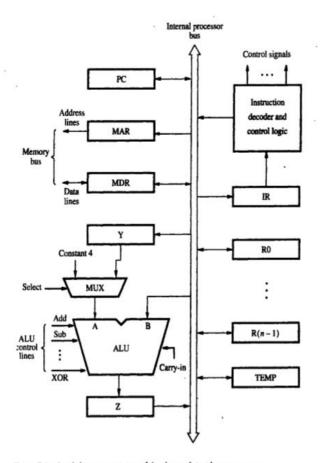


Figure 7.1 Single-bus organization of the datapath inside a processor.

2. Describe the sequence of control signals to be generated to fetch an instruction from memory in a single bus organization.

Sequence-5 M

| Step | Action   |
|------|--|
| 1    | PCout, MARin, Read, Select4, Add, Zin              |
| 2    | $Z_{out}$ , $PC_{in}$ , $Y_{in}$ , $WMFC$          |
| 3    | MDR <sub>out</sub> , IR <sub>in</sub>              |
| 4    | R3 <sub>out</sub> , MAR <sub>in</sub> , Read       |
| 5    | R1out, Yin, WMFC                                   |
| 6    | MDR <sub>out</sub> , SelectY, Add, Z <sub>in</sub> |
| 7    | Zout, Rlin, End                                    |
|      | A  |

Figure 7.6 Control sequence for execution of the instruction Add (R3),R1.

3. Explain the organization of a complete processor, with the help of a block Diagram.

Diagram-5 M

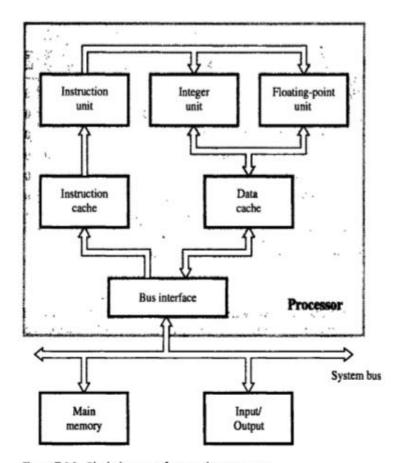


Figure 7.14 Block diagram of a complete processor.

4. With a neat diagram, discuss three bus organization of CPU. Compare the performance with single-bus organization.

Diagram-5 M

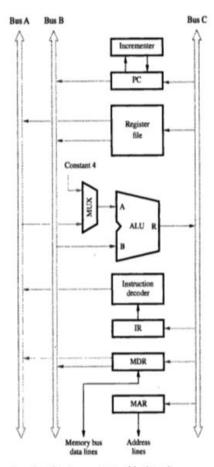


Figure 7.8 Three-bus organization of the datapath.

5. Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z in control signal.

Diagrams- 5 M

Figure 7.11 Separation of the decoding and encoding functions

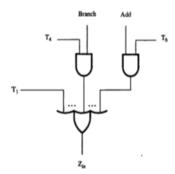


Figure 7.12 Generation of the Z<sub>ix</sub> control signal for the processor in Figure 7.1.

6. Write a microroutine for any conditional branching instruction(with suitable comments) w.r.t Microprogrammed control.

Microroutine-5 M

| Address  | Microinstruction   |  |
|--|--|--|
| 0  | PCout, MARin, Read, Select4, Add, Zin                              |  |
| 1  | $\mathbf{Z}_{out}$ , $\mathbf{PC}_{in}$ , $\mathbf{Y}_{in}$ , WMFC |  |
| 2  | $\mathrm{MDR}_{out},\mathrm{IR}_{in}$                              |  |
| 3  | Branch to starting address of appropriate microroutine             |  |
|  |  |  |
| 25   | If $N=0$ , then branch to microinstruction 0                       |  |
| 26   | Offset-field-of- $IR_{out}$ , SelectY, Add, $Z_{in}$               |  |
| 27   | $\mathbf{Z}_{out}$ , $\mathbf{PC}_{in}$ , $\mathbf{End}$           |  |
| THE R ART IS AN EXCHANGE THE MARKET THE MARK |  |  |

Figure 7.17 Microroutine for the instruction Branch < 0.

7. With a block diagram, describe the organization of a microprogrammed control unit.

Diagram-5 M

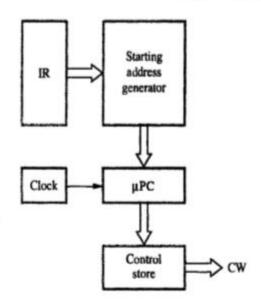


Figure 7.16 Basic organization of a microprogrammed control unit.