IAT 3 SOLUTION

Sub:	VLSI Design							Code:	18EC72
Date:	25 / 01/ 2022	Duration:	90 mins	Max Marks:	50	Sem:	VII	Branch:	ECE

1. Explain any five latch circuits.

Answer:

Figure a) shows a very simple transparent latch built from a single transistor. It is compact and fast but suffers four limitations. The output does not swing from *rail-to-rail* (i.e., from GND to V_{DD}); it never rises above $V_{DD} - V_t$. The output is also *dynamic*; in other words, the output floats when the latch is opaque. If it floats long enough, it can be disturbed by leakage. *D* drives the *diffusion input* of a pass transistor directly, leading to potential noise issues and making the delay harder to model with static timing analyzers. Finally, the state node is *exposed*, so noise on the output can corrupt the state. The remainder of the figures illustrate improved latches using more transistors to achieve more robust operation.

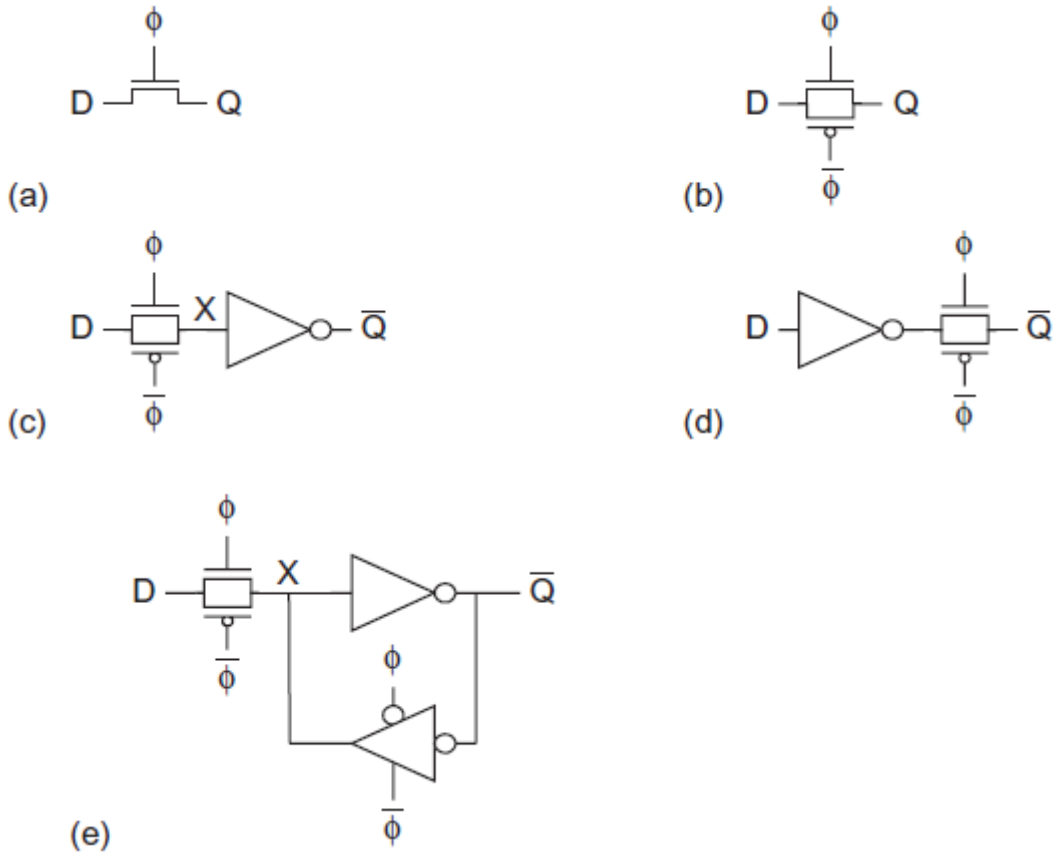


Figure b) uses a CMOS transmission gate in place of the single nMOS pass transistor to offer rail-to-rail output swings. It requires a complementary clock ϕ, which can be provided as an additional input or locally generated from ϕ through an inverter. Figure c) adds an output inverter so that the state node *X* is isolated from noise on the output. Of course, this creates an inverting latch. Figure d also behaves as an inverting latch with a buffered input but unbuffered output. The inverter followed by a transmission gate is essentially equivalent to a tristate inverter but has a slightly lower logical effort because the output is driven by both transistors of the transmission gate in parallel. Figure c) and d) are both fast dynamic latches. In modern processes, subthreshold leakage is large enough that dynamic nodes retain their values for only a short time, especially at the high temperature and voltage encountered during burn-in test. Therefore, practical latches need to be staticized, adding feedback to prevent the output from floating, as shown in Figure e). When the clock is 1, the input transmission gate is ON, the feedback tristate is OFF, and the latch is transparent. When the clock is 0, the input transmission gate turns OFF. However, the feedback tristate turns ON, holding *X* at the correct level.

1. With circuit diagram, explain the logic '1' and '0' transfer using pass transistor logic.

Answer

The fundamental building block of nMOS dynamic logic circuits, consisting of an nMOS pass transistor driving the gate of another nMOS transistor, is shown in Fig. 1. As

pass transistor MP is driven by the periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion-load nMOS inverter obviously assumes a logic-low or a logic-high level, depending on the voltage V_x.

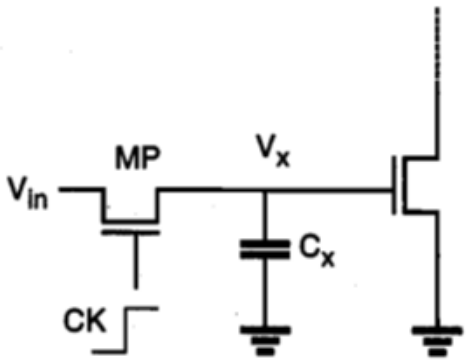


Figure 1. The basic building block for nMOS dynamic logic, which consists of an nMOS pass transistor driving the gate of another nMOS transistor.

the pass transistor MP provides the only current path to the intermediate capacitive node (soft node) X. When the clock signal becomes inactive (CK = 0), the pass transistor ceases to conduct and the charge stored in the parasitic capacitor C_x continues to determine the output level of the inverter.
charge-up event.

Logic "1" Transfer

Assume that the soft node voltage is equal to 0 initially, i.e., $V_x(t = 0) = 0$ V. A logic "1" level is applied to the input terminal, which corresponds to $V_{in} = V_{OH} = V_{DD}$. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at $t = 0$. It can be seen that the pass transistor MP starts to conduct as soon as the clock signal becomes active and that MP will operate in saturation throughout this cycle since $V_{DS} = V_{GS}$. Consequently, $V_{DS} > V_{GS} - V_{T,n}$. The circuit to be analyzed for the logic "1" transfer event can be simplified into an equivalent circuit as shown in Fig. 2.

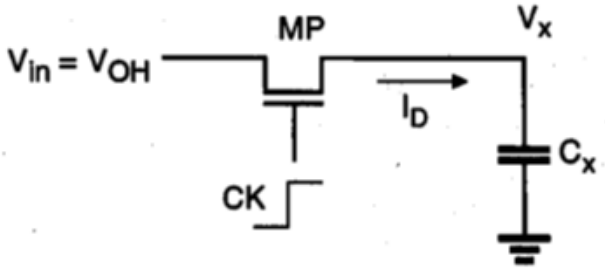


Figure 2. Equivalent circuit for the logic "1" transfer event.

The pass transistor MP operating in the saturation region starts to charge up the capacitor C_x, thus,

$$C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(V_{DD} - V_x - V_{T,n}\right)^2 \qquad (1)$$

Note that the threshold voltage of the pass transistor is actually subject to substrate bias effect and therefore, depends on the voltage level V_x. To simplify our analysis, we will neglect the substrate bias effect at this point. Integrating (1), we obtain

$$\int_0^t dt = \frac{2C_x}{k_n}\int_0^{V_x} \frac{dV_x}{\left(V_{DD} - V_x - V_{T,n}\right)^2}$$

$$= \frac{2C_x}{k_n}\left(\frac{1}{\left(V_{DD} - V_x - V_{T,n}\right)}\right)\Bigg|_0^{V_x} \qquad (2)$$

$$t = \frac{2C_x}{k_n}\left[\left(\frac{1}{V_{DD} - V_x - V_{T,n}}\right) - \left(\frac{1}{V_{DD} - V_{T,n}}\right)\right] \qquad (3)$$

This equation can be solved for $V_x(t)$, as follows.

$$V_x(t) = \left(V_{DD} - V_{T,n}\right)\frac{\left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}{1 + \left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t} \qquad (4)$$

The variation of the node voltage V_x according to (4) is plotted as a function of time in Fig. 3. The voltage rises from its initial value of 0 V and approaches a limit value for large t, but it cannot exceed its limit value of $V_{max} = (V_{DD} - V_{T,n})$. The pass transistor will turn off when $V_x = V_{max}$, since at this point, its gate-to-source voltage will be equal to its threshold voltage. Therefore, the voltage at node X can never attain the full power supply voltage level of V_{DD} during the logic "1" transfer. The actual value of the maximum possible voltage V_{max} at node X can be found by taking into account the substrate bias effect for MP.

$$V_{max} = V_x\big|_{t\to\infty} = V_{DD} - V_{T,n}$$

$$= V_{DD} - V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max}} - \sqrt{|2\phi_F|}\right) \qquad (5)$$

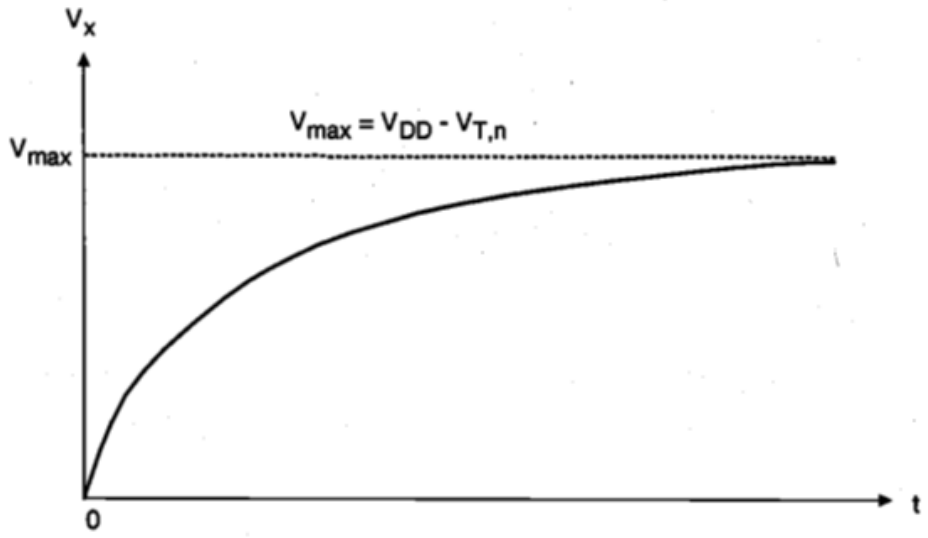


Figure 3. Variation of V_x as a function of time during logic "1" transfer.

Thus, the voltage V_x which is obtained at node X following a logic "1" transfer can be considerably lower than V_{DD}. Also note that the rise time of the voltage V_x will be *underestimated* if the zero-bias threshold voltage V_{T0} is used in (3). In that case, the actual charge-up time will be longer than predicted by (3), because the drain current of the nMOS transistor is decreased due to the substrate bias effect.

Logic "0" Transfer

Assume that the soft-node voltage V_x is equal to a logic "1" level initially, i.e., $V_x(t = 0) = V_{max} = (V_{DD} - V_{T,n})$. A logic "0" level is applied to the input terminal, which corresponds to $V_{in} = 0$ V. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at $t = 0$. The pass transistor MP starts to conduct as soon as the clock signal becomes active, and the direction of drain current flow through MP will be opposite to that during the charge-up (logic "1" transfer) event. This means that the intermediate node X will now correspond to the drain terminal of MP and that the input node will correspond to its source terminal. With $V_{GS} = V_{DD}$ and $V_{DS} = V_{max}$, it can be seen that the pass transistor operates in the linear region throughout this cycle, since $V_{DS} < V_{GS} - V_{T,n}$.

The circuit to be analyzed for the logic "0" transfer event can be simplified into an equivalent circuit as shown in Fig. 6. As in the logic "1" transfer case, the depletion-load nMOS inverter does not affect this event.

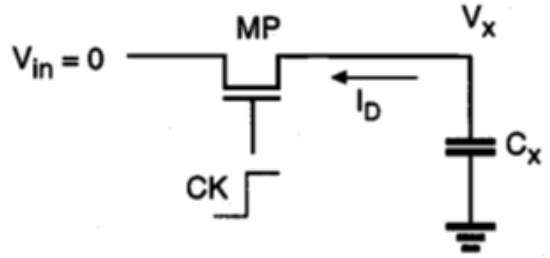


Figure 6. Equivalent circuit for the logic "0" transfer event.

The pass transistor MP operating in the linear region discharges the parasitic capacitor C_x, as follows:

$$-C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2\right) \qquad (7)$$

$$dt = -\frac{2C_x}{k_n} \cdot \frac{dV_x}{2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2} \qquad (8)$$

Note that the source voltage of the nMOS pass transistor is equal to 0 V during this event; hence, there is no substrate bias effect for MP ($V_{T,n} = V_{T0,n}$). But the initial condition $V_x(t=0) = (V_{DD} - V_{T,n})$ contains the threshold voltage *with* substrate bias effect, because the voltage V_x is set during the preceding logic "1" transfer event. To simplify the expressions, we will use $V_{T,n}$ in the following. Integrating both sides of (8) yields

$$\int_0^t dt = -\frac{2C_x}{k_n} \int_{V_{DD}-V_{T,n}}^{V_x} \left(\frac{\frac{1}{2\left(V_{DD} - V_{T,n}\right)}}{2\left(V_{DD} - V_{T,n}\right) - V_x} + \frac{\frac{1}{2\left(V_{DD} - V_{T,n}\right)}}{V_x} \right) dV_x \qquad (9)$$

$$t = \frac{C_x}{k_n\left(V_{DD} - V_{T,n}\right)} \left[\ln\left(\frac{2\left(V_{DD} - V_{T,n}\right) - V_x}{V_x} \right) \right] \Bigg|_{V_{DD}-V_{T,n}}^{V_x} \qquad (10)$$

Finally, the fall-time expression for the node voltage V_x can be obtained as

$$t = \frac{C_x}{k_n\left(V_{DD} - V_{T,n}\right)} \ln\left(\frac{2\left(V_{DD} - V_{T,n}\right) - V_x}{V_x} \right) \qquad (11)$$

The variation of the node voltage V_x according to (11) is plotted as a function of time in Fig. 7. It is seen that the voltage drops from its logic-high level of V_{max} to 0 V. Hence, unlike the charge-up case, the applied input voltage level (logic 0) can be transferred to the soft node without any modification during this event.

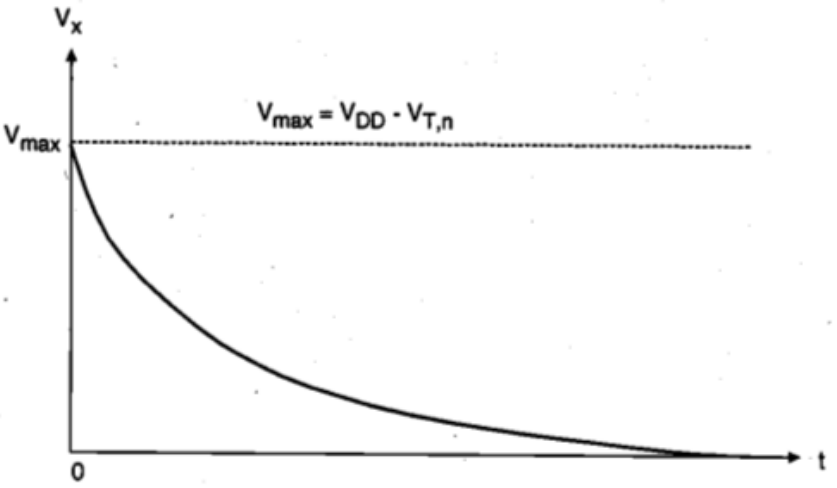


Figure 7. Variation of V_x as a function of time during logic "0" transfer.

The fall time (τ_{fall}) for the soft-node voltage V_x can be calculated from (11) as follows. First, define the two time points $t_{90\%}$ and $t_{10\%}$ as the times at which the node voltage is equal to 0.9 V_{max} and 0.1 V_{max}, respectively. These two time points can easily be found by using (11).

$$t_{90\%} = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{(2-0.9)\left(V_{DD}-V_{T,n}\right)}{0.9\left(V_{DD}-V_{T,n}\right)}\right)$$
$$= \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{1.1}{0.9}\right) \qquad (12)$$

$$t_{10\%} = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{1.9}{0.1}\right) \qquad (13)$$

The fall time of the soft-node voltage V_x is by definition the difference between $t_{10\%}$ and $t_{90\%}$, which is found as

$$\tau_{fall} = t_{10\%} - t_{90\%}$$
$$= \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\ln(19)-\ln(1.22)\right]$$
$$= 2.74\frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)} \qquad (14)$$

2. Explain the structure of dynamic CMOS logic circuits. Explain the cascading problem associated with dynamic CMOS logic.

Answer: A dynamic CMOS circuit technique allows us to significantly reduce the number of transistors used to implement any logic function. The circuit operation is based on first *precharging* the output node capacitance and subsequently, *evaluating* the output level according to the applied inputs. Both of these operations are scheduled by a single clock signal, which drives one nMOS and one pMOS transistor in each dynamic stage. A dynamic CMOS logic gate which implements the function $F = \overline{(A_1A_2A_3 + B_1B_2)}$ is shown in Fig1 below.

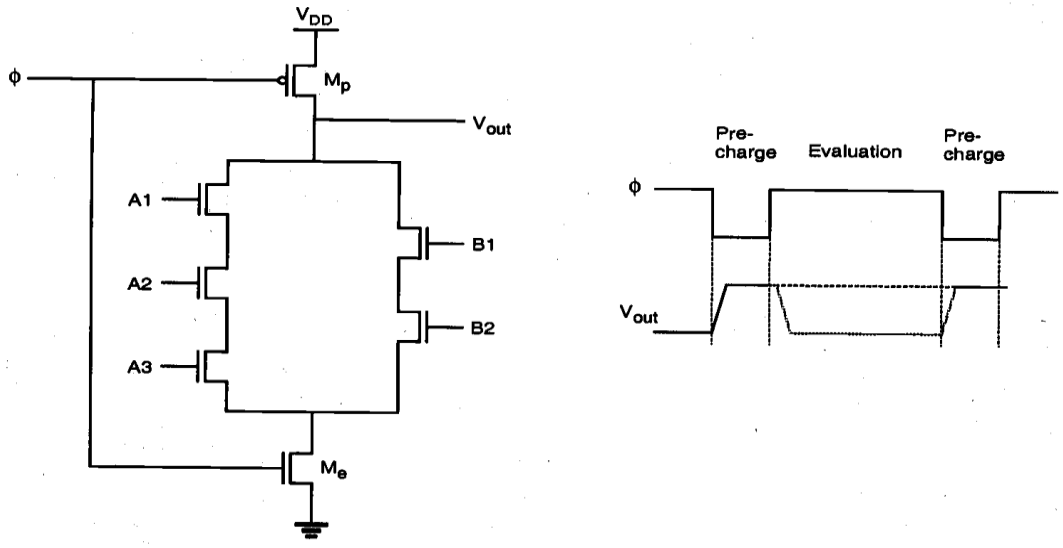


Figure 1. Dynamic CMOS logic gate implementing a complex Boolean function.

When the clock signal is low (precharge phase), the pMOS precharge transistor Mp is conducting, while the complementary nMOS transistor Me is off. The parasitic output capacitance of the circuit is charged up through the conducting pMOS transistor to a logic-high level of Vout = *VDD*. The input voltages are also applied during this phase, but
they have no influence yet upon the output level since Me is turned off. When the clock signal becomes high (evaluate phase), the precharge transistor Mp turns off and Me turns on. The output node voltage may now remain at the logic- high level or drop to a logic low, depending on the input voltage levels. If the input signals create a conducting path between the output node and the ground, the output capacitance will discharge toward *VOL* = 0 V. The final discharged output level depends on the time span of the evaluation phase. Otherwise, V_{out} remains at *VDD*.

For practical multi-stage applications, however, the dynamic CMOS gate presents a significant problem. To examine this fundamental limitation, consider the two-stage
cascaded structure shown in Fig.2 below. Here, the output of the first dynamic CMOS stage drives one of the inputs of the second dynamic CMOS stage, which is assumed to be a two input NAND gate for simplicity.

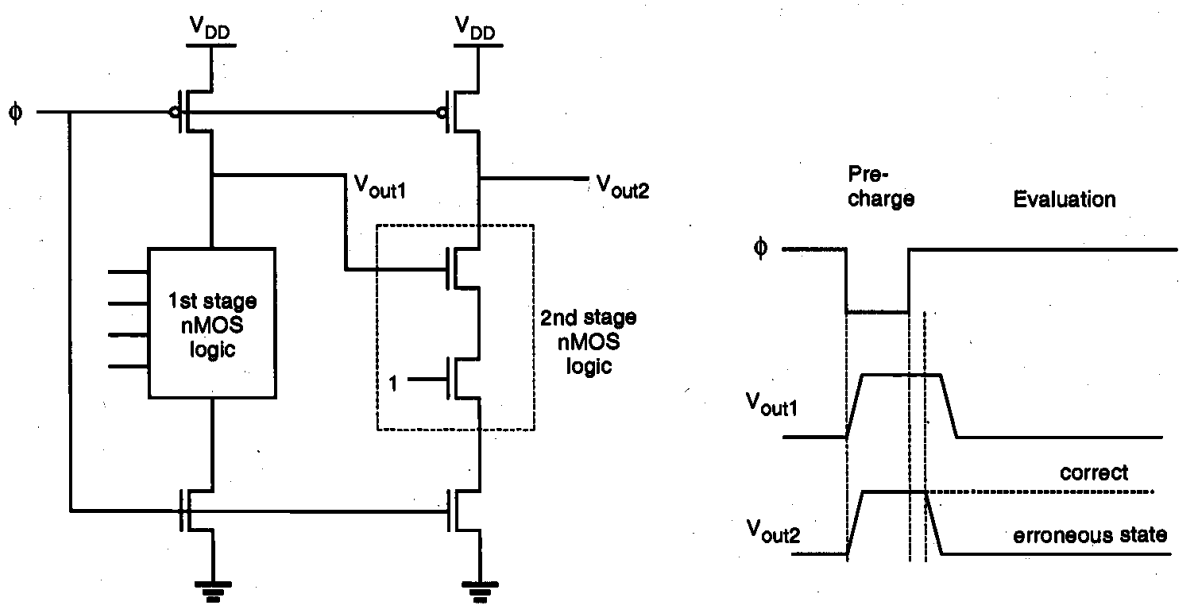
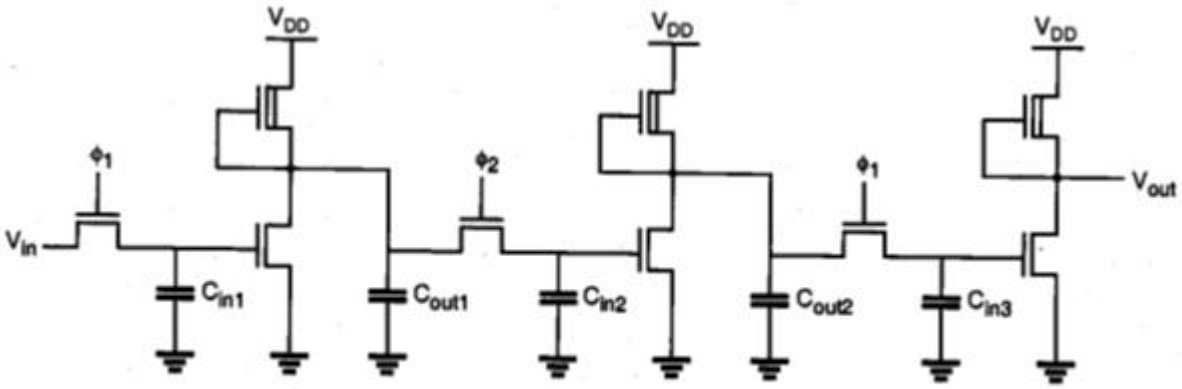


Figure 2. Illustration of the cascading problem in dynamic CMOS logic.

During the precharge phase, both output voltages Vout1 and *Vout2* are pulled up by the respective pMOS precharge devices. Also, the external inputs are applied during this phase. The input variables of the first stage are assumed to be such that the output Vout1 will drop to logic "0" during the evaluation phase. On the other hand, the external input of the second-stage NAND2 gate is assumed to be a logic " 1," as shown in Fig. 2. When the evaluation phase begins, both output voltages Vout1 and *Vout2* are logic-high. The output of the first stage (Voutl) eventually drops to its correct logic level after a certain time delay. However, since the evaluation in the second stage is done concurrently, starting with the high value of V_{out1} at the beginning of the evaluation phase, the output voltage *Vout2* at the end of the evaluation phase will be *erroneously* low. Although the first stage output subsequently assumes its correct output value once the stored charge is drained, the correction of the second-stage output is not possible.

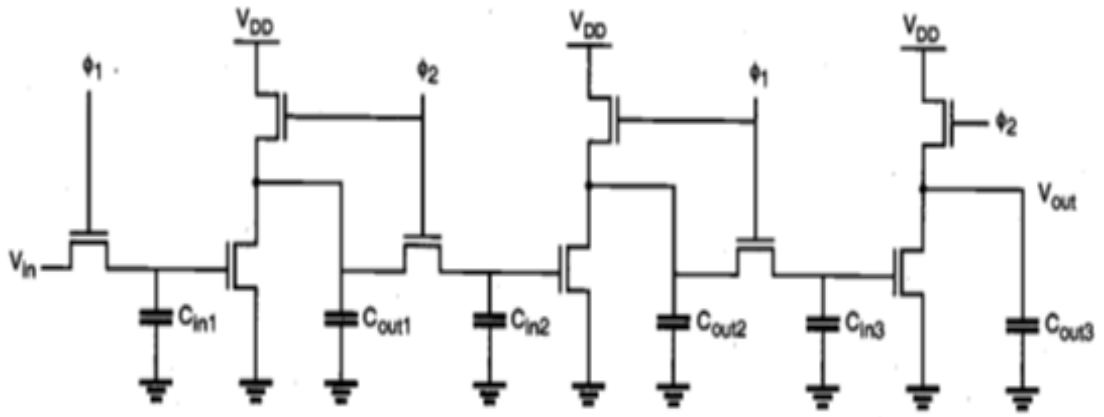
3. Explain the depletion-load and enhancement mode dynamic shift register circuits.

Answer:



Three stages of a depletion-load nMOS dynamic shift register circuit driven with two-phase clocking.

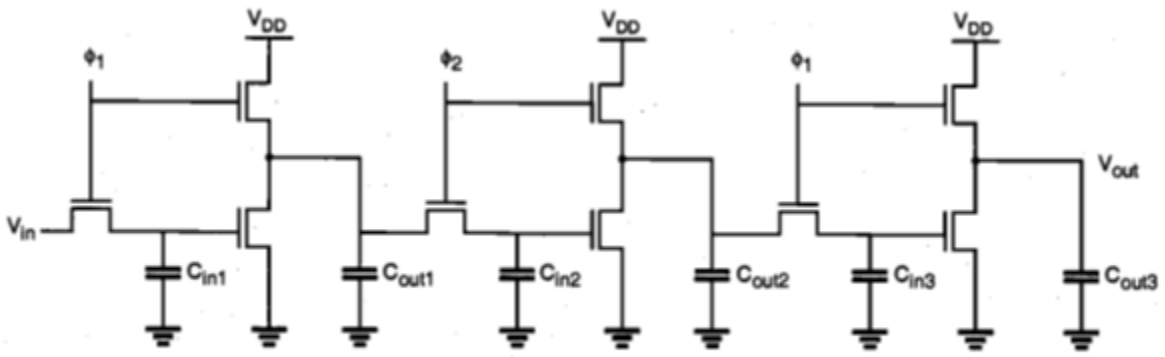
The operation of the shift register circuit is as follows. During the active phase of ϕ1 the input voltage level V is transferred into the input capacitance Cin1. Thus, the valid output voltage level of the first stage is determined as the inverse of the current input during this cycle. When ϕ2 becomes active during the next phase, the output voltage level of the first stage is transferred into the second stage input capacitance *Cin 2*, and the valid output voltage level of the second stage is determined. During the active ϕ2 phase, the first-stage input capacitance continues to retain its previous level via charge storage. When ϕ1 becomes active again, the original data bit *written* into the register during the previous cycle is transferred into the third stage, and the first stage can now accept the next data bit.



Enhancement-load dynamic shift register (ratioed logic).

When ϕ1 is active, the input voltage level *Vi.* is transferred into the first-stage input capacitance CinI through the pass transistor. In this phase, the enhancement-type nMOS load transistor of the first-stage inverter is not active yet. During the next phase (active *ϕ2),* the load transistor is turned on. Since the input logic level is still being preserved in *Cin1,* the output of the first inverter stage attains its valid logic level. At the same time, the input pass transistor of the second stage is also turned on, which allows this newly determined output level to be transferred into the input capacitance Cin 2 of the second stage. When clock Al becomes active again, the valid output level across *Cin2* is determined, and transferred into *Cin3*. Also, a new input level can be accepted *(pipelined)* into Cin1, during this phase. In this circuit, the valid low-output voltage level *VOL* of each stage is strictly determined by the driver-to-load ratio, since the output pass transistor (input pass transistor of next stage) turns on in phase with the load transistor. Therefore, this circuit arrangement is also called *ratioed dynamic logic.*

Next, consider the second dynamic enhancement-load shift register implementation where, in each stage, the input pass transistor and the load transistor are driven by the same clock phase.

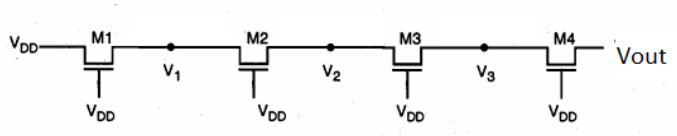


Enhancement-load dynamic shift register (ratioless logic).

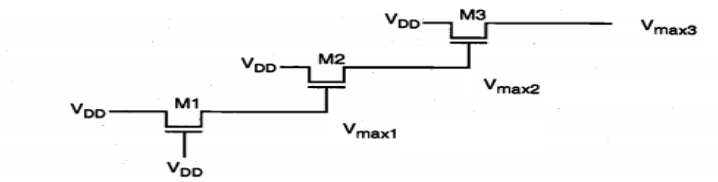
When ϕ1 is active, the input voltage level *Vin* is transferred into the first-stage input capacitance *Cin1*, through the pass transistor. Note that at the same time, the enhancement type nMOS load transistor of the first-stage inverter is active. Therefore, the output of the first inverter stage attains its valid logic level. During the next phase (active ϕ*2*), the input pass transistor of the next stage is turned on, and the logic level is transferred onto the next stage. Here, we have to consider two cases, as follows. If the output level across *Cout,1* is logic-high at the end of the active ϕ1 phase, this voltage level is transferred to Cout2 via charge sharing over the pass transistor during the active ϕ*2* phase. Note that the logic-high level at the output node is subject to threshold voltage drop, i.e., it is one threshold voltage lower than the power supply voltage. To correctly transfer a logic-high level after charge sharing, the ratio of the capacitors (*Cout,*/Cin) must be made large enough during circuit design. If, on the other hand, the output level of the first stage is logic-low at the end of the active ϕl phase, then the output capacitor *Cout1* will be completely drained to a voltage of *VOL* = 0 V when ϕ1 turns off. This can be achieved because a logic-high level is being stored in the input capacitance *Cin1* in this case, which forces the driver transistor to remain in conduction. Obviously, the logic-low level of *VOL* = 0 V is also transferred into the next stage via the pass transistor during the active ϕ*2* phase. When clock ϕ1, becomes active again, the valid output level across Cout 2 is determined and transferred into Cin3. Also, a new input level can be accepted into Cin1, during this phase. Since the valid logic-low level of *VOL* = 0 V can be achieved regardless of the driver-to-load ratio, this circuit arrangement is called *ratioless dynamic logic.*

4. If $Vdd = 5\,V$ and threshold voltage of all the nmos devices in the circuit is $1V$, then Find

1. **V1, V2, V3** and **Vout** for the following circuit

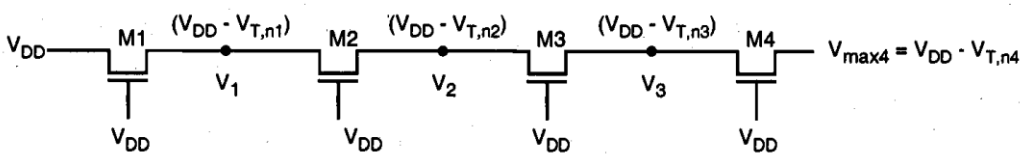


2. **Vmax1, Vmax2 andVmax3** for the circuit shown below.



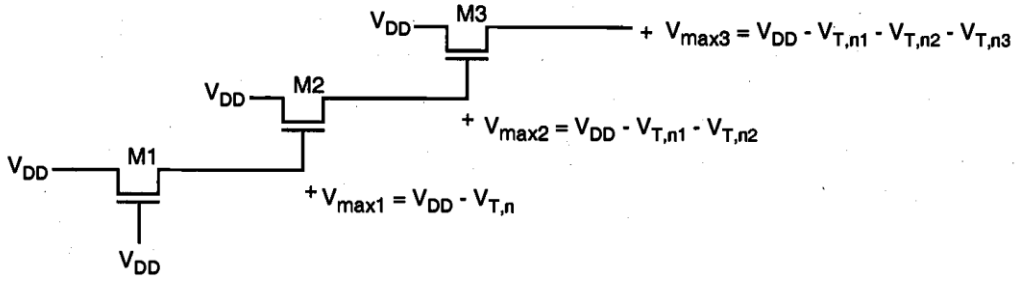
Solution:

1. We know,



Therefore, V1=V2=V3=Vout= 5V-1V=4V

2. We know,



Therefore, Vmax1=5-1=4V, Vmax2=5-1-1=3V, Vmax3=5-1-1-1=2V

5. **Explain the charge storage and charge leakage concepts associated with the pass transistor diffusion terminal driving the gate of another transistor**.

assume that a logic-high voltage level has been transferred to the soft node during the active clock phase and that now both the input voltage V_{in} and the clock are equal to 0 V. The charge stored in C_x will gradually leak away, primarily due to the leakage currents associated with the pass transistor. The gate current of the inverter driver transistor is negligible for all practical purposes.

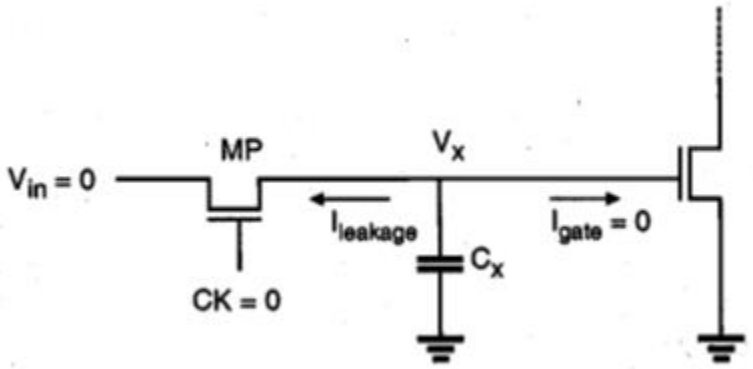


Figure 8. Charge leakage from the soft node.

Figure 9 shows a simplified cross-section of the nMOS pass transistor, together with the lumped node capacitance C_x. We see that the leakage current responsible for draining the soft-node capacitance over time has two main components, namely, the subthreshold channel current and the reverse conduction current of the drain-substrate junction.

$$I_{leakage} = I_{subthreshold(MP)} + I_{reverse(MP)} \qquad (15)$$

Note that a certain portion of the total soft-node capacitance C_x is due to the reverse biased drain-substrate junction, which is also a function of the soft-node voltage V_x. Other components of C_x, which are primarily due to oxide-related parasitics, can be considered constants. In our analysis, these constant capacitance components will be represented by C_{in} (Fig. 10). Thus, we have to express the total charge stored in the soft node as the sum of two main components, as follows.

$$Q = Q_j(V_x) + Q_{in} \quad \text{where} \quad Q_{in} = C_{in} \cdot V_x$$

$$C_{in} = C_{gb} + C_{poly} + C_{metal} \qquad (16)$$

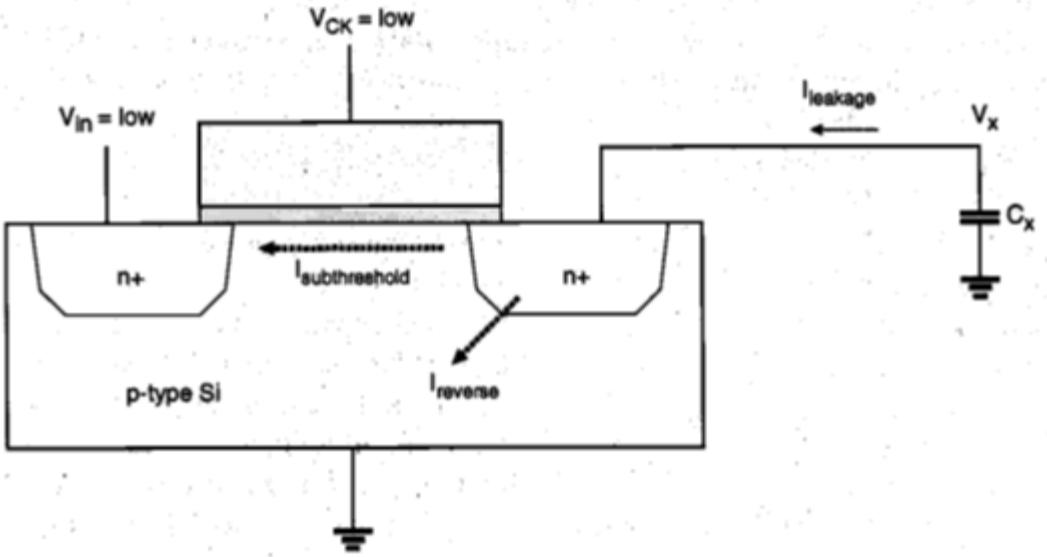


Figure 9. Simplified cross-section of the nMOS pass transistor, showing the leakage current components responsible for draining the soft-node capacitance C_x.

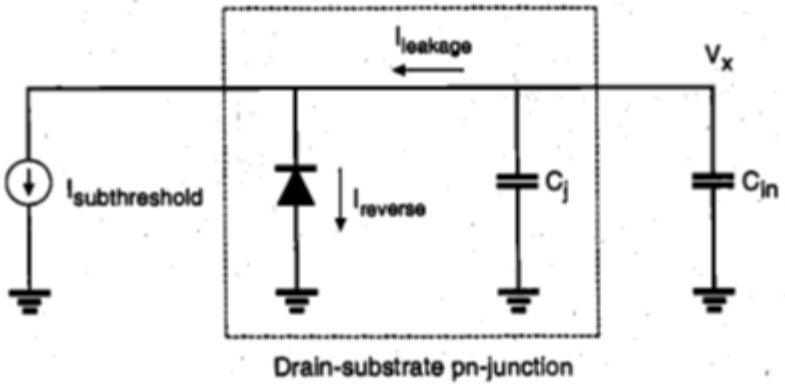


Figure 10. Equivalent circuit used for analyzing the charge leakage process.

The total leakage current can be expressed as the time derivative of the total soft-node charge Q.

$$\begin{aligned} I_{leakage} &= \frac{dQ}{dt} \\ &= \frac{dQ_j(V_x)}{dt} + \frac{dQ_{in}}{dt} \\ &= \frac{dQ_j(V_x)}{dV_x}\frac{dV_x}{dt} + C_{in}\frac{dV_x}{dt} \end{aligned} \qquad (17)$$

where

$$\frac{dQ_j(V_x)}{dV_x} = C_j(V_x) = \frac{A \cdot C_{j0}}{\sqrt{1 + \frac{V_x}{\phi_0}}} = A \cdot \sqrt{\frac{q\,\varepsilon_{Si}\,N_A}{2(\phi_0 + V_x)}} \qquad (18)$$

$$\phi_0 = \frac{kT}{q} \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right) \qquad (19)$$

$$C_{j0} = \sqrt{\frac{q\,\varepsilon_{Si}\,N_A\,N_D}{2(N_A + N_D)\phi_0}} \approx \sqrt{\frac{q\,\varepsilon_{Si}\,N_A}{2\,\phi_0}} \qquad (20)$$

Also note that the subthreshold current in deep-submicron transistors can significantly exceed the reverse conduction current, especially for $V_{DS} = V_{DD}$. In long-channel transistors, the magnitude of the subthreshold current can be comparable to that of the reverse leakage current. The reverse conduction current in turn has two main components, the constant reverse saturation current I_0, and the generation current I_{gen} which originates in the depletion region and is a function of the applied bias voltage V_x.

To estimate the actual charge leakage time from the soft node, we have to solve the differential equation given in (17), taking into account the voltage-dependent capacitance components and the nonlinear leakage currents. For a quick estimate of the worst-case leakage behavior, on the other hand, the problem can be further simplified.

Assume that the *minimum* combined soft-node capacitance is given as

$$C_{x,min} = C_{gb} + C_{poly} + C_{metal} + C_{db,min} \qquad (21)$$

where $C_{db,min}$ represents the minimum junction capacitance, obtained under the bias condition $V_x = V_{max}$. Now we define the *worst-case holding time* (t_{hold}) as the shortest time required for the soft-node voltage to drop from its initial logic-high value to the logic threshold voltage due to leakage. Once the soft-node voltage reaches the logic threshold, the logic stage being driven by this node will lose its previously held state.

$$t_{hold} = \frac{\Delta Q_{critical,min}}{I_{leakage,max}} \qquad (22)$$

where

$$\Delta Q_{critical,min} = C_{x,min}\left(V_{max} - \frac{V_{DD}}{2}\right) \qquad (23)$$

6. Explain the operation of 3-T DRAM cell.

Answer:

The circuit diagram of a typical three-transistor dynamic RAM cell is shown in Fig. 1 as well as the column pull-up (precharge) transistors and the column read/write circuitry. Here, the binary information is stored in the form of charge in the parasitic node capacitance C_1. The storage transistor M2 is turned on or off depending on the charge stored in C_1, and the pass transistors M1 and M3 act as access switches for data read and write operations. The cell has two separate bit lines for "data read" and "data write," and two separate word lines to control the access transistors.

The operation of the three-transistor DRAM cell and its peripheral circuitry is based on a two-phase non-overlapping clock scheme. The precharge events are driven by ϕ_1, whereas the "read" and "write" events are driven by ϕ_2. Every "data read" and "data write" operation is preceded by a precharge cycle, which is initiated with the precharge signal PC going high. During the precharge cycle, the column pull-up transistors are activated, and the corresponding column capacitances C_2 and C_3 are charged up to logic-high level. With typical enhancement type nMOS pull-up transistors ($V_{T0} \approx 1.0$ V) and a power supply voltage of 5 V, the voltage level of both columns after the precharge is approximately equal to 3.5 V.

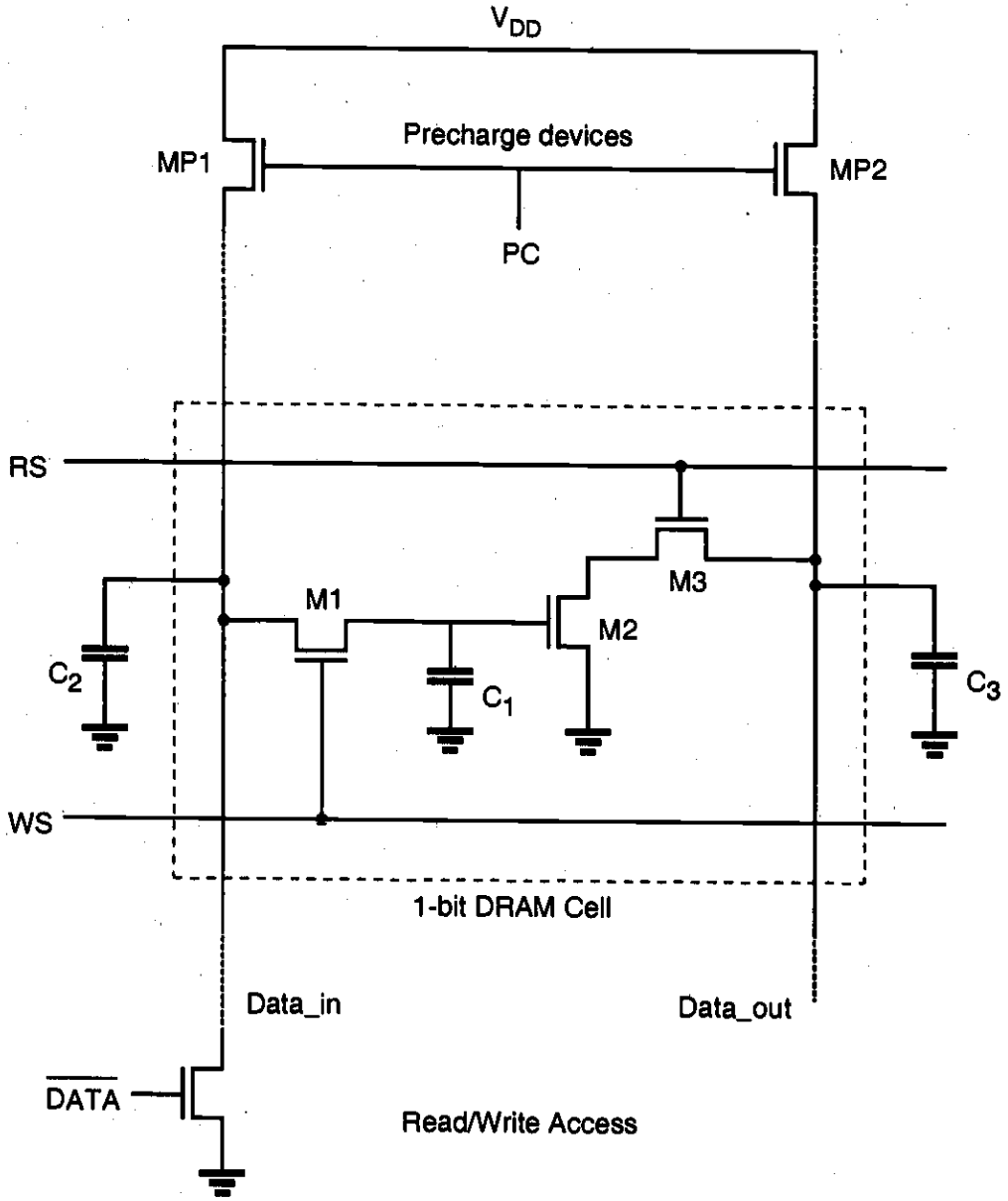


Figure 1: Three-transistor DRAM cell with the pull-up and read/write circuitry.

All "data read" and "data write" operations are performed during the active ϕ_2 phase, i.e., when PC is low. Figure 2 depicts the typical voltage waveforms associated with the 3-T DRAM cell during a sequence of four consecutive operations: write "1," read "1," write "0," and read "0." The four precharge cycles shown in Fig. 2 are numbered 1, 3, 5, and 7, respectively. Figure 3 illustrates the transient currents charging up the two columns (D_{in} and D_{out}) during a precharge cycle. The precharge cycle is effectively completed when both capacitance voltages reach their steady-state values. Note here that the two column capacitances C_2 and C_3 are at least one order of magnitude larger than the internal storage capacitance C_1.

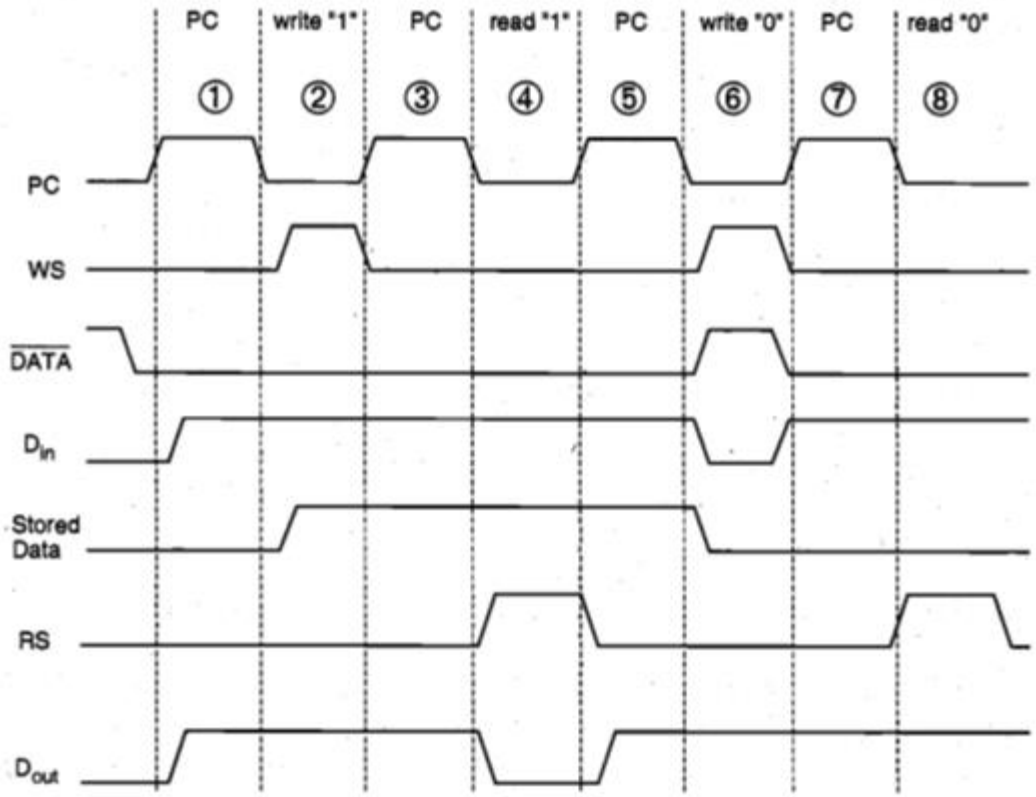


Figure 2 Typical voltage waveforms associated with the 3-T DRAM cell during four consecutive operations: write "1," read "1," write "0," and read "0."

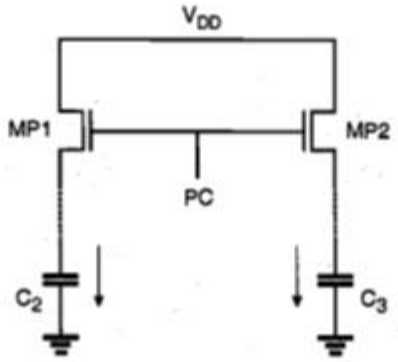


Figure 3 . Column capacitances C_2 and C_3 are being charged-up through MP1 and MP2 during the precharge cycle.

For the write "1" operation, the *inverse* data input is at the logic-low level, because the data to be written onto the DRAM cell is logic "1." Consequently, the "data write" transistor MD is turned off, and the voltage level on column D_{in} remains high. Now, the "write select" signal WS is pulled high during the active phase of ϕ_2. As a result, the write access transistor M1 is turned on. With M1 conducting, the charge on C_2 is now shared

with C_1 (Fig. 4). Since the capacitance C_2 is very large compared to C_1, the storage node capacitance C_1 attains approximately the same logic-high level as the column capacitance C_2 at the end of the charge-sharing process.

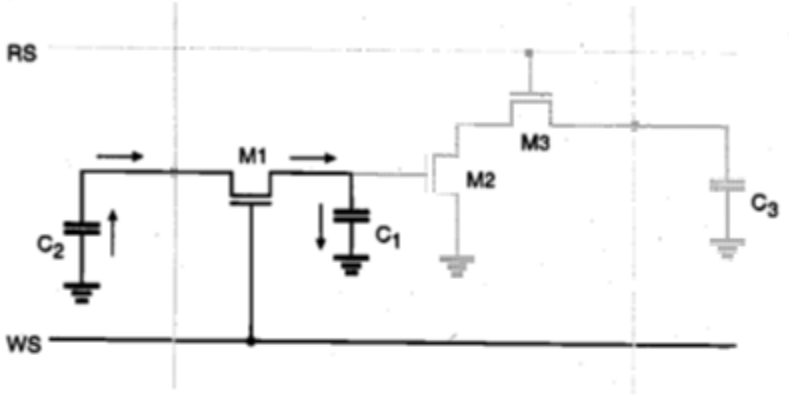


Figure 4 . Charge sharing between C_2 and C_1 during the write "1" sequence.

After the write "1" operation is completed, the write access transistor M1 is turned off. With the storage capacitance C_1 charged-up to a logic-high level, transistor M2 is now conducting. In order to read this stored "1," the "read select" signal RS must be pulled high during the active phase of ϕ_2, following a precharge cycle. As the read access transistor M3 turns on, M2 and M3 create a conducting path between the "data read" column capacitance C_3 and the ground. The capacitance C_3 discharges through M2 and M3, and the falling column voltage is interpreted by the "data read" circuitry as a stored logic "1." The active portion of the DRAM cell during the read "1" cycle is shown in Fig. 5 . Note that the 3-T DRAM cell may be read repeatedly in this fashion without disturbing the charge stored in C_1.

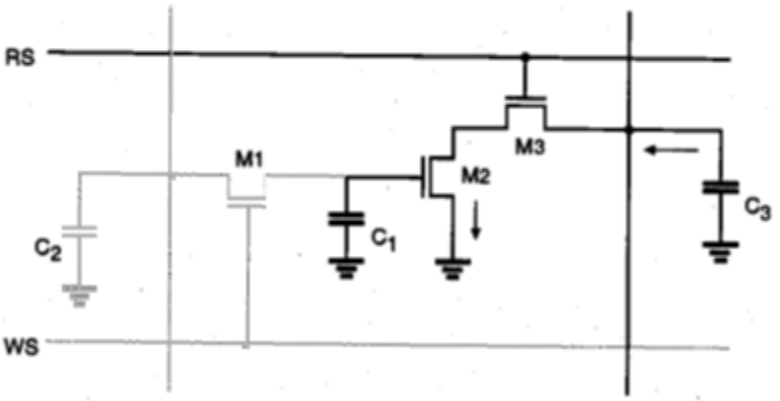


Figure 5 . The column capacitance C_3 is discharged through the transistors M2 and M3 during the read "1" operation.

For the write "0" operation, the inverse data input is at the logic-high level, because the data to be written onto the DRAM cell is a logic "0." Consequently, the data write

transistor is turned on, and the voltage level on column D_{in} is pulled to logic "0." Now, the "write select" signal WS is pulled high during the active phase of ϕ_2. As a result, the write access transistor M1 is turned on. The voltage level on C_2, as well as that on the storage node C_1, is pulled to logic "0" through M1 and the data write transistor, as shown in Fig. 6 . Thus, at the end of the write "0" sequence, the storage capacitance C_1 contains a very low charge, and the transistor M2 is turned off since its gate voltage is approximately equal to zero.

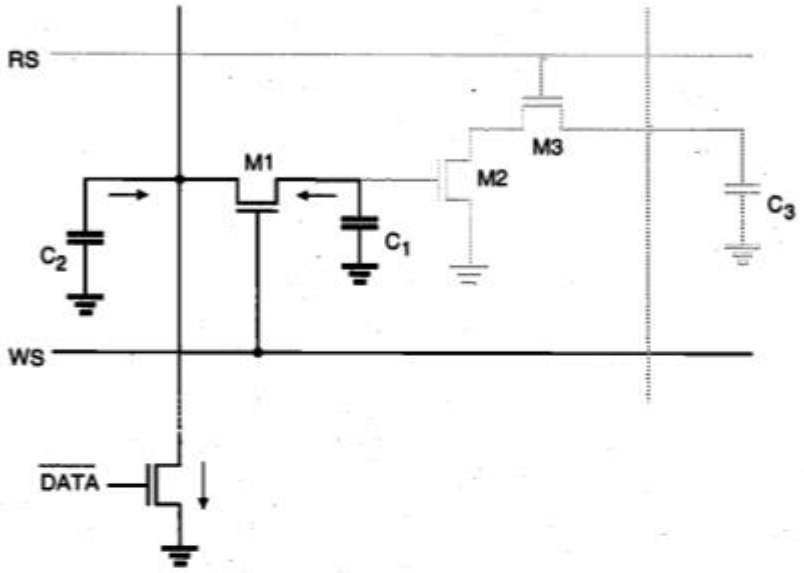


Figure 6 . Both C_1 and C_2 are discharged via M1 and the data write transistor during the write "0" sequence.

In order to read this stored "0," the "read select" signal RS must be pulled high during the active phase of ϕ_2, following a precharge cycle. The read access transistor M3 turns on, but since M2 is off, there is no conducting path between the column capacitance C_3 and the ground (Fig. 7). Consequently, C_3 does not discharge, and the logic-high level on the D_{out} column is interpreted by the data read circuitry as a stored "0" bit.

As we already pointed out in the beginning of this section, the charge stored in C_1 cannot be held indefinitely, even though the "data read" operations do not significantly disturb the stored charge. The drain junction leakage current of the write access transistor M1 is the main reason for the gradual depletion of the stored charge on C_1. In order to *refresh* the data stored in the DRAM cells before they are altered due to leakage, the data must be periodically read, inverted (since the data output level reflects the inverse of the stored data), and then written back into the same cell location. This refresh operation is performed for all storage cells in the DRAM array every 2 to 4 ms. Note that all bits in one row can be refreshed at once, which significantly simplifies the procedure.

It can be seen that the three-transistor dynamic RAM cell examined here does not dissipate any static power for data storage, since there is no continuous current flow in the circuit. Also, the use of periodic precharge cycles instead of static pull-up further reduces the dynamic power dissipation. The additional peripheral circuitry required for

scheduling the non-overlapping control signals and the refresh cycles does not significantly overshadow these advantages of the low-power dynamic memory.

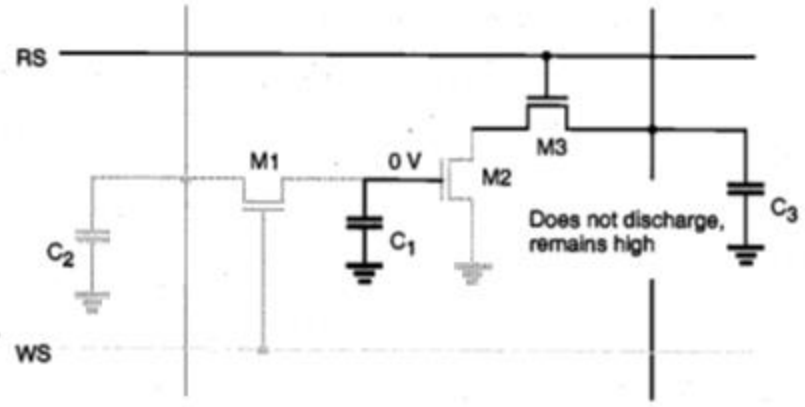


Figure 7. The column capacitance C_3 cannot discharge during the read "0" cycle.

7. Explain the operation of 1-T DRAM cell.

Answer:

The circuit diagram of the one-transistor (1-T) DRAM cell consisting of one explicit storage capacitor and one access transistor is shown in Fig. 1 . Here, C_1 represents the storage capacitor which typically has a value of 30 to 100 fF. Similar to the 3-T DRAM cell, binary data are stored as the presence or absence of charge in the storage capacitor. Capacitor C_2 represents the much larger parasitic column capacitance associated with the word line. Charge sharing between this large capacitance and the very small storage capacitance plays a very important role in the operation of the 1-T DRAM cell.

The "data write" operation on the 1-T cell is quite straightforward. For the write "1" operation, the bit line (D) is raised to logic "1" by the write circuitry, while the selected word line is pulled high by the row address decoder. The access transistor M1 turns on, allowing the storage capacitor C_1 to charge up to a logic-high level. For the write "0" operation, the bit line (D) is pulled to logic "0" and the word line is pulled high by the row address decoder. In this case, the storage capacitor C_1 discharges through the access transistor, resulting in a stored "0" bit.

In order to read stored data out of a 1-T DRAM cell, on the other hand, we have to build a fairly elaborate read-refresh circuit. The reason for this is the fact that the "data read" operation on the one-transistor DRAM cell is by necessity a "destructive readout." This means that the stored data must be destroyed or lost during the read operation. Typically, the read operation starts with precharging the column capacitance C_2. Then, the word line is pulled high in order to activate the access transistor M1. Charge sharing between C_1 and C_2 occurs and, depending on the amount of stored charge on C_1, the column voltage either increases or decreases slightly. Note that charge sharing inevitably destroys the stored charge on C_1. Hence, we also have to *refresh* data every time we perform a "data read" operation.

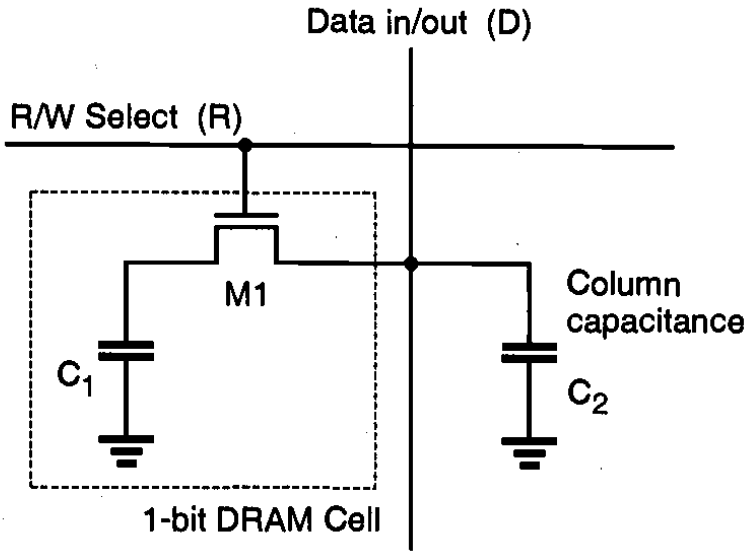


Figure 1:Typical one-transistor (1-T) DRAM cell with its access lines.

The "read-refresh" operation occurs in three stages. First, the precharge devices are turned on during the active phase of PC. Both column capacitances C_D and $C_{\overline{D}}$ are charged-up to the same logic-high level, whereas the dummy nodes X and Y are pulled to logic-low level. The devices involved in the precharge operation are highlighted in Fig. 2 . Note that during this phase, all other signals are inactive.

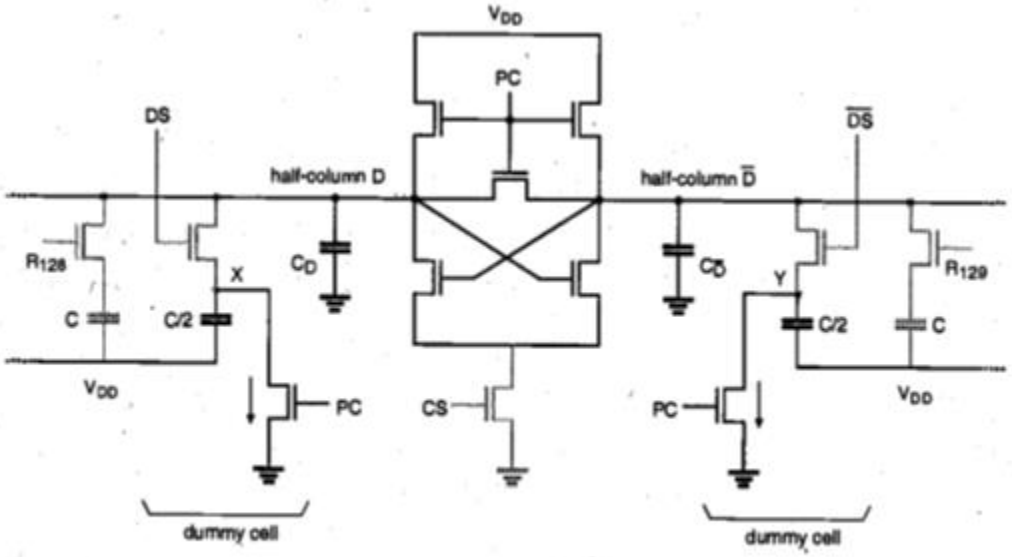


Figure 2 . The half-columns are being charged-up during the precharge phase.

Next, one of the 256 word lines is raised to logic "1" during the row selection phase. At the same time, the dummy cell on the other side is also selected by raising either *DS* or $\overline{DS}$. This situation is depicted in Fig. 3 , where only the selected

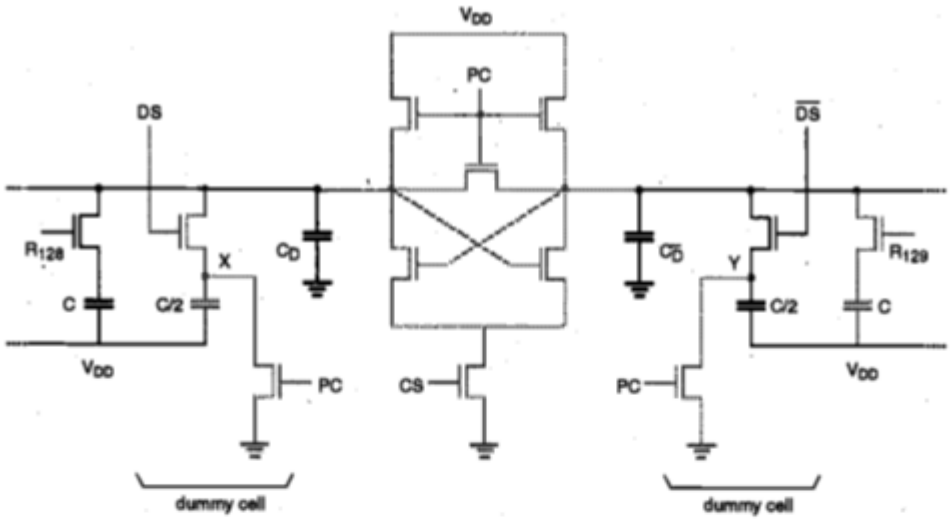


Figure 3 . Two complementary column voltages are determined through charge sharing, on the one side between the selected storage cell and the half-column capacitance, on the other side between the dummy cell and the other half-column capacitance.

DRAM cell (left) and the corresponding dummy cell (right) are highlighted. If a logic "1" is stored in the selected cell, the voltage on the half-column *D* will rise slightly, while the voltage on half-column $\overline{D}$ drops, because the dummy cell is being charged up. If a logic "0" is stored in the selected cell, however, the voltage on the half-column *D* will also drop, and the drop in V_D will be larger than the drop in $V_{\overline{D}}$. Consequently, there will be a detectable difference between a stored "0" and a stored "1."

The final stage of the "read-refresh" operation is performed during the active phase of CS, the column-select signal. As soon as the cross-coupled latch is activated, the slight voltage difference between the two half-columns is amplified, and the latch forces the two half-columns into opposite states (Fig. 4). Thus, the stored data on the selected DRAM cell is refreshed while it is being read by the "read-refresh" circuitry.

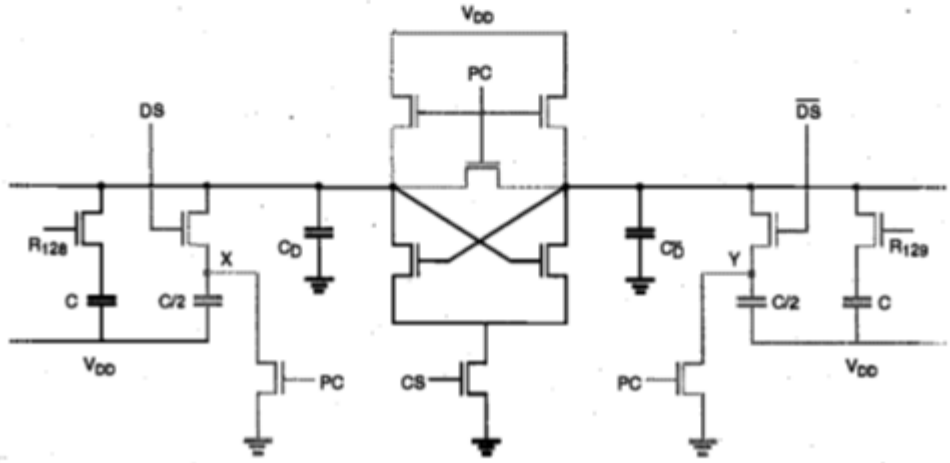


Figure 4 . The cross-coupled latch circuit is used for detection of the voltage difference between the half-columns and for restoring the voltage level on the accessed cell.