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Internal Assesment Test - II

Sub:	**DIGITAL SYSTEM DSESIGN**							Code:	18EE35
Date:	25/01/2022	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	EEE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Explain the operation of the SR latch acting as a switch debouncer with the help of a timing diagram.	10	CO3	L2
2	Convert a JK flip-flop to T flip-flop D flip-flop and SR flip-flop with necessary procedures and diagrams.	10	CO3	L2
3	Explain the working of a master slave JK flip-flop with a neat logic diagram, function table, logic symbol and timing diagram along with waveforms. What is race around condition? How to overcome race around condition?	10	CO3	L2
4	With a neat logic diagram, explain the 4-bit universal shift register using D-flip-flop and a 4:1 MUX. Write a mode control and register operation.	10	CO3	L2

P.T.O

CCI

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CCI

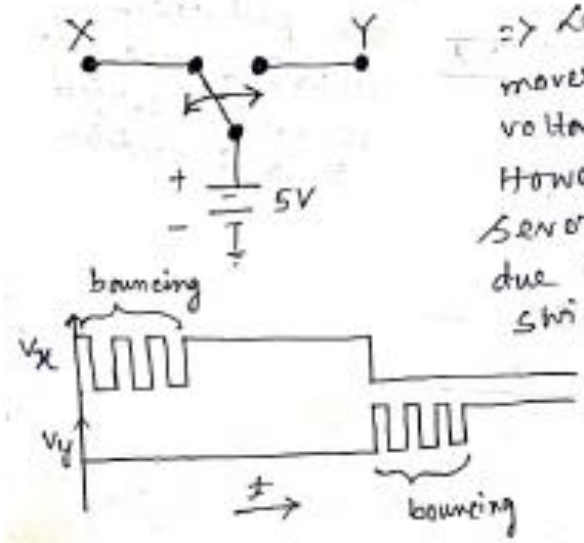
P.T.O

5	esign a synchronous counter with counting sequence 0,2,6,1,3,7,0. .....using JKFF	10	CO3	L3
6	Design a Mod 10 ripple counter using JK flip-flop and Differentiate synchronous and asynchronous counter.	10	CO3	L3

5	Design a synchronous counter with counting sequence 0,2,6,1,3,7,0. ....using JKFF	10	CO3	L3
6	Design a Mod 10 ripple counter using JK flip-flop and Differentiate synchronous and asynchronous counter.	10	CO3	L3

1.

Sol^n:- push button switches are used in the digital system for interfacing. When mechanical switches such as toggle switches or push buttons are switched from one position to the other, several make and break operations occur at the second position called switch bounce. Thus, reading taken during bouncing period may be faulty.



=> Let us assume, when the switch moves from Y to X, the voltage across Y becomes zero. However, when it touches X, several make and break happen due to the 'spring like nature of switch. A similar action takes place when the switch moves from X to Y.

2.

3.11.4 JK Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in Table 3.11.5.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-map simplification

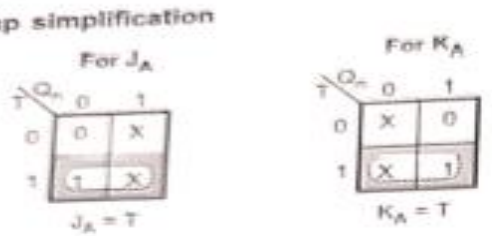


Fig. 3.11.8

Logic diagram

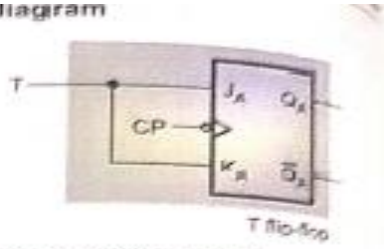


Fig. 3.11.9 JK to T flip-flop conversion

3.11.5 JK Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 3.11.6.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Table 3.11.6

K-map simplification

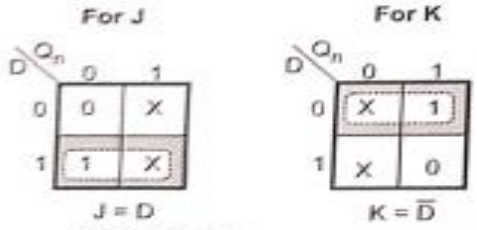


Fig. 3.11.10

Logic diagram

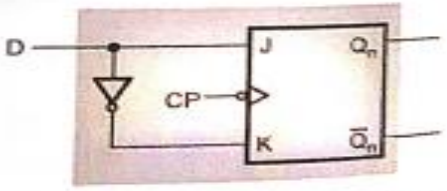


Fig. 3.11.11 JK to D flip-flop conversion

3.11.8 JK Flip-Flop to SR Flip-Flop

The excitation table for above conversion is as shown in Table 3.11.10.

Inputs		Present state	Next state	Flip-flop inputs	
S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

Table 3.11.10 Excitation table for JK to SR conversion

K-map simplification

For J

SR \ Q_n	0	1
00	0	X
01	0	X
11	X	X
10	1	X

J = S

For K

SR \ Q_n	0	1
00	X	0
01	X	1
11	X	X
10	0	X

K = R

Fig. 3.11.17

Logic diagram

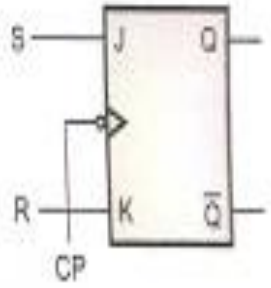
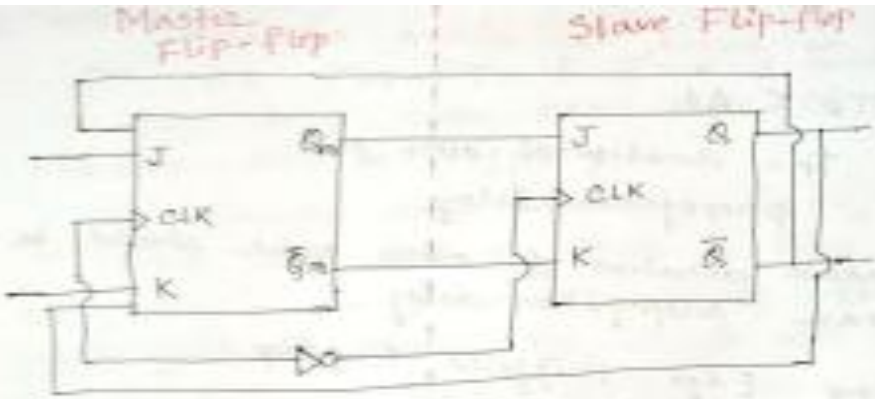


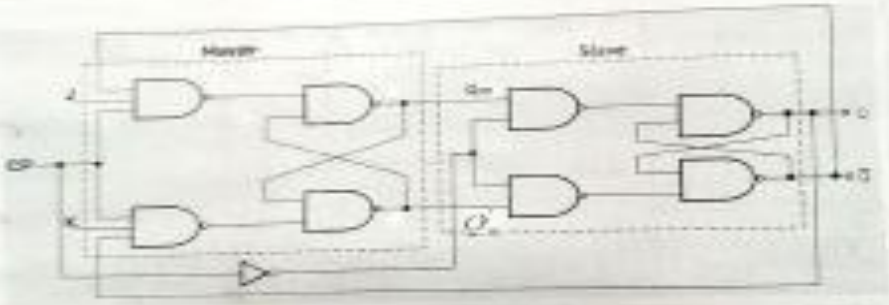
Fig. 3.11.18 JK to SR

3.

=> The Master-Slave JK Flip-flop is basically a combination of two JK Flipflops connected together in series configuration. Out of these, one acts as the 'Master' and another acts as 'Slave'. The output from the Master flip-flop is connected to the two inputs of the Slave flip flop whose outputs are feedback to the inputs of Master Flip-flop

In addition, the circuit also includes an inverter which is connected to the clock pulse. When clock is high, Master will be activated and when clock is low, Slave will be activated.





As shown in the above Figure, clock signal is connected ~~through~~ directly to the Master Flip flop, but it is connected through an inverter to the slave Flip-flop Therefore, the information present at the J and K inputs is transmitted to the output of Master flip-flop on the positive clock pulse and it is held there until the negative clock pulse occurs, after which it is allowed to pass through the output of Slave Flip-flop

Case :- I

When J = 1 and K = 0, the Master sets on the positive clock. The high $\bar{Q}_m$ output of the master drives the J input of the slave, so at negative clock slave sets, copying the action of the Master.

Case :- II

When J = 0 and K = 1, the master resets on the positive clock. The high $\bar{Q}_m$ output of the master goes to the K input of the slave. Thus, at the negative clock slave resets, again copying the action of the master.

Case :- III

When J = K = 1, master toggles on the positive clock and slave then copies the output of master on the negative clock.

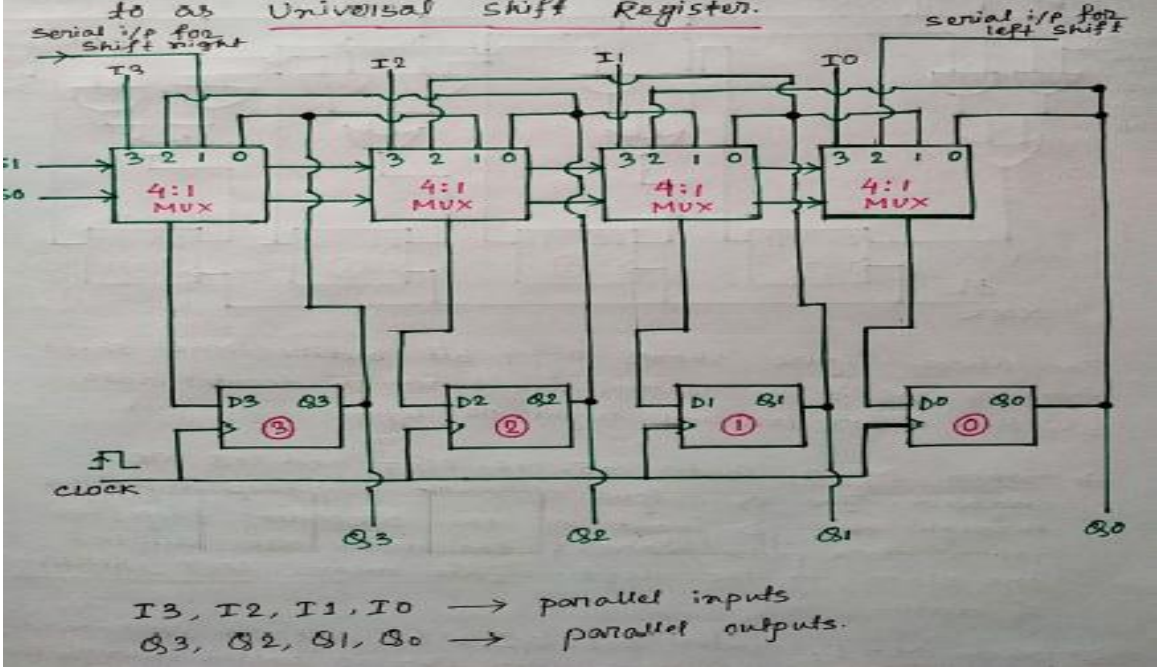
Case :- IV

When J = K = 0, the output of master remains same at the positive clock pulse. Thus the output of slave also remains same at the negative clock pulse. The Truth Table is given below

CLK	J	K	Q_{n+1}
⎍	0	0	Q_n (no change)
⎍	0	1	0 (Reset)
⎍	1	0	1 (set)
⎍	1	1	$\bar{Q}_n$ (Toggle)

4.

⇒ If a Register has both left shift and right shift and also parallel load capabilities, it is referred to as Universal Shift Register.



I3, I2, I1, I0 ⟶ parallel inputs

Q3, Q2, Q1, Q0 ⟶ parallel outputs.

→ 91 consists of 4 flip flops and 4 Multiplexers. The four Multiplexers have two common select inputs S1 and S0. and they select appropriate input for D flip-flop. The below table shows the register operation depending on the select lines of multiplexer.

Mode Control		Register Operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	parallel Load.

→ When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in Register value.

→ When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift Register.

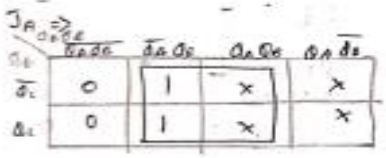
→ When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift Register.

→ Finally when $S_1S_0 = 11$, the binary information on the parallel input lines is transfered into the register simultaneously and. it is a parallel load operation.

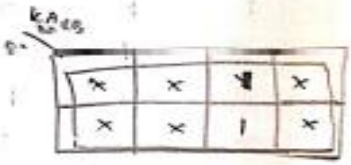
5.

Present state			Next state			$(JK)_A$		$(JK)_B$		$(JK)_C$	
Q_A	Q_B	Q_C	Q_{An+1}	Q_{Bn+1}	Q_{Cn+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	0	1	1	0	x	1	x	x	0
0	1	0	1	1	0	1	x	x	0	0	x
0	1	1	1	1	1	1	x	x	0	x	0
1	0	0	x	x	x	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	0	0	1	x	1	x	1	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

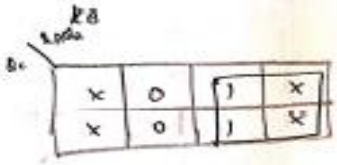


$J_A \Rightarrow Q_B$

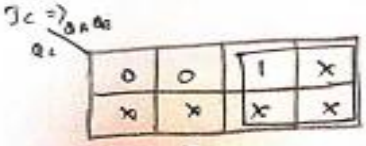


$K_A = 1$

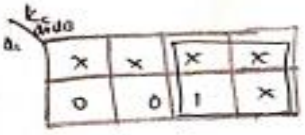
$J_B = 1$



$K_B = Q_A$



$J_C = Q_A$



$K_C = Q_A$

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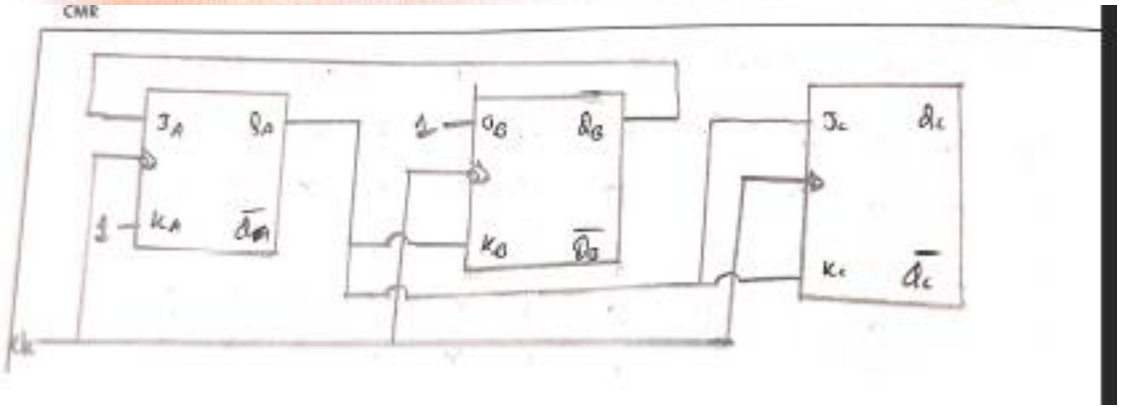
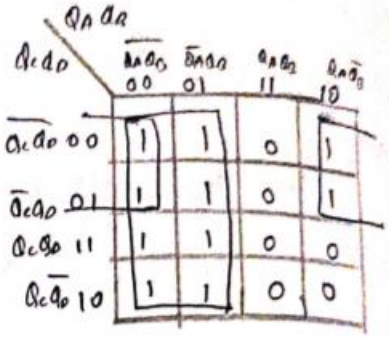


6.

Q_A	Q_B	Q_C	Q_D	Reset
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



Reset $\Rightarrow \overline{Q_A} + \overline{Q_B}\,\overline{Q_C}$