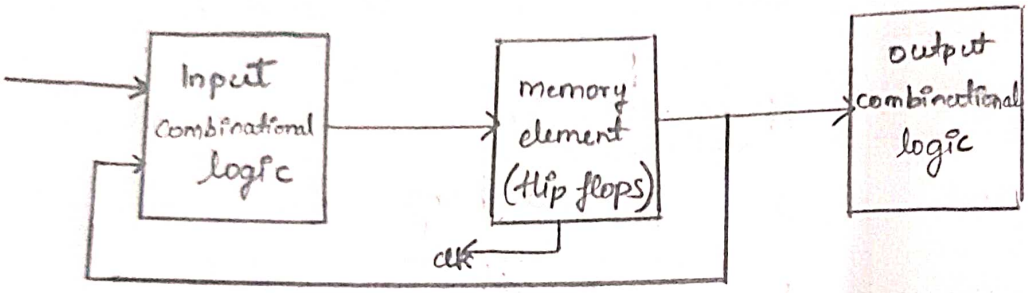
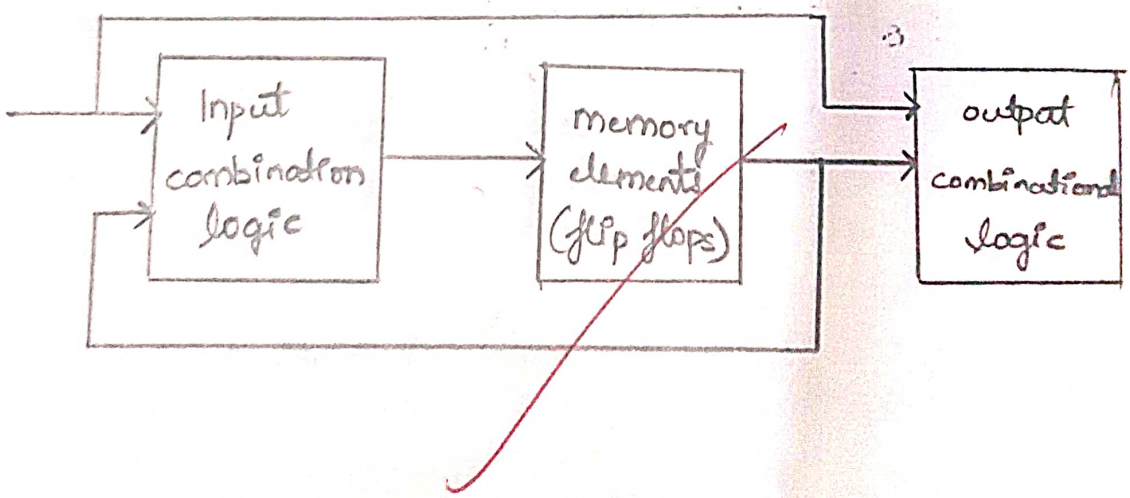
CMR

Internal Assessment Test - III

1) Moore : when the output of the sequential circuit is depend on the only present state of sequential circuit it is known as moore model.

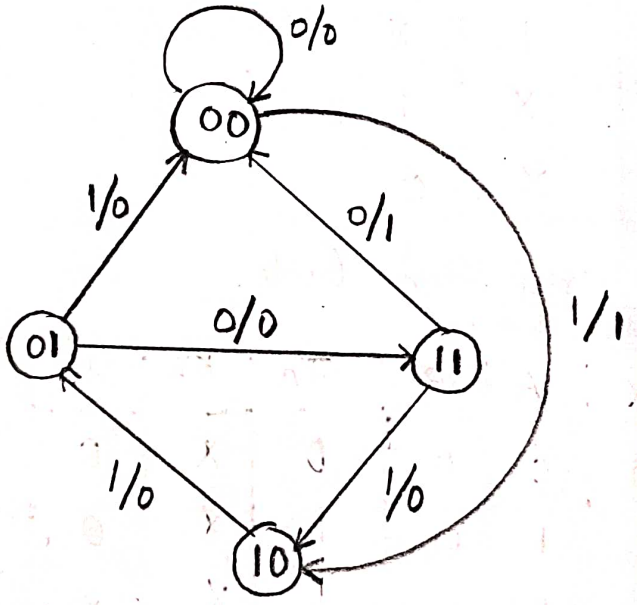


Mealy model: when the output of the sequential circuit is depend on the both present state and inputs of sequential circuit it is known as mealy model.



Moore model.	Mealy model.
i) Its output function is depend on the present state.	i) Its output function is depend on both present and input states.
ii) Inputs will not effect the function of output.	iii) Inputs will effect the function of output.
iii) Number of ~~states~~ state requi-red to implementing the same function is more.	iii) less number of states required for implementing the same function.

3)



No of flip flop required ⇒ 4 states ⇒ 2^2 = 2 flip flops.

Step 1:

Write the state table.

Present stage		Next stage				output	
A	B	x=0		x=1		x=0	x=1
		A	B	A	B		
0	0	0	0	1	0	0	1
0	1	1	1	0	0	0	0
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0

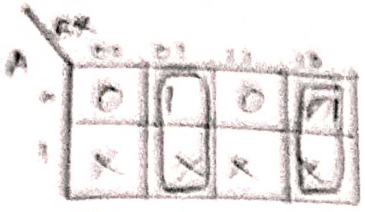
step2: write excitation table of JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

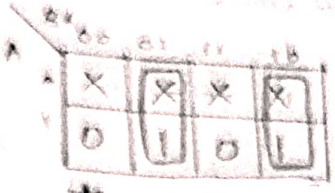
step 3: write transition table.

Present stage		Next stage						output	
A	B	X	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

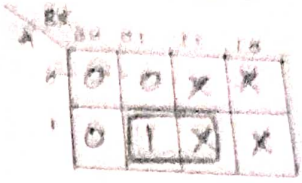
step 4: write the K-map



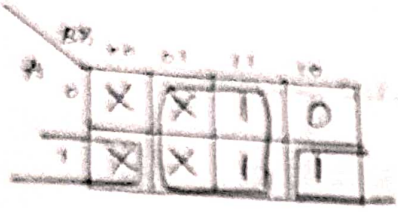
$J_A = \bar{B}X + B\bar{X}$
$= B \oplus X$



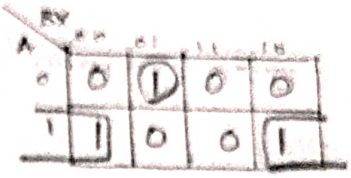
$K_A = B \oplus X$



$J_B = AX$

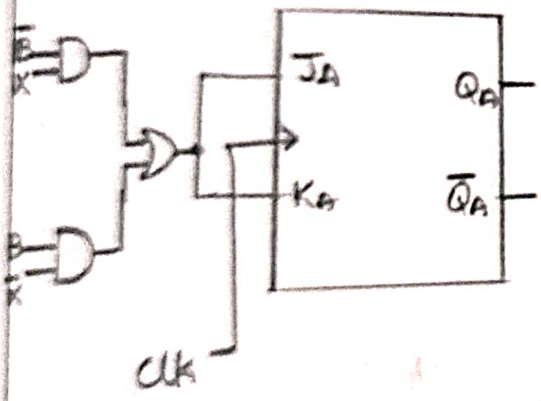


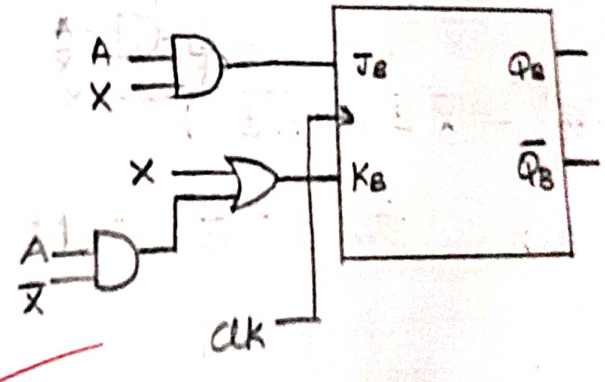
~~$K_B = B +$~~
$K_B = X + A\bar{X}$

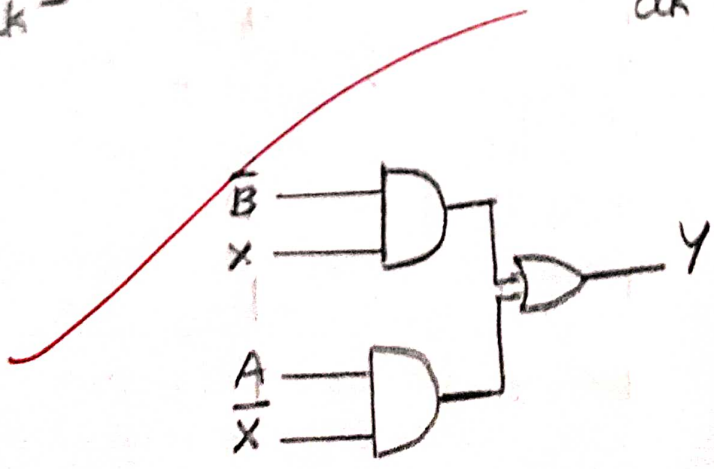


$Y = \bar{B}X + A\bar{X}$

step 5: draw sequential circuit.







4)

step 1: write equations

$J_A = B$ $\quad J_B = \bar{X}$

$K_A = \bar{X}B$ $\quad K_B = A \oplus X$

$F = A \oplus B$

step 2: write transition equations,

$JK \Rightarrow Q^+ = J\bar{Q} + \bar{K}Q$

$Q_A^+ = J_A \bar{Q}_A + \bar{K}_A Q_A$

$= B\bar{Q}_A + \overline{\bar{X}B} \cdot Q_A$

$= B\bar{Q}_A + (X + \bar{B})QA$

$= B\bar{A} + (X + \bar{B})A$

$Q_B^+ = J_B \bar{Q}_B + \bar{K}_B Q_B$

$= \bar{X}\bar{Q}_B + \overline{(A \oplus X)} Q_B$

$Q_B^+ = \bar{X}\bar{B} + \overline{(A \oplus X)} B$

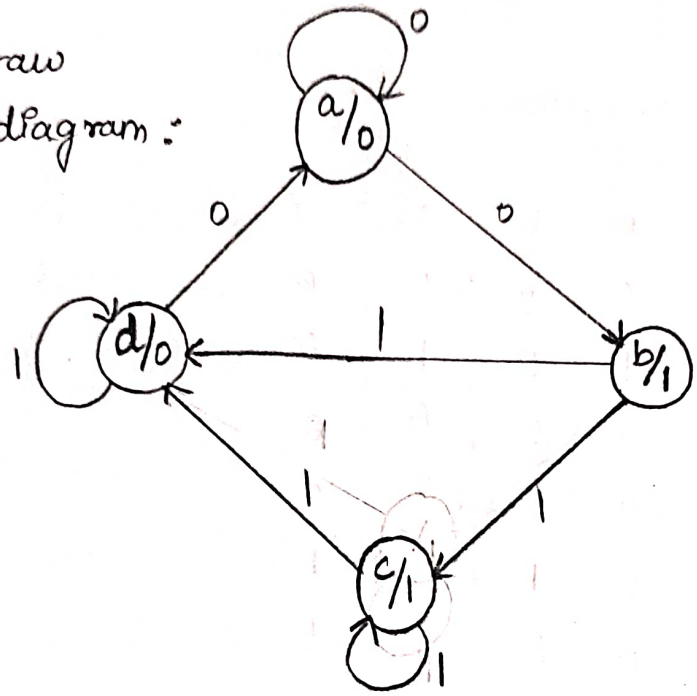
step 3: write state table.

Present stage		Next State				output
A	B	$x=0$		$x=1$		$Y = A \oplus B$
		A	B	A	B	
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

draw state table:

Present state	Next state		output
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

step 5: draw state diagram:



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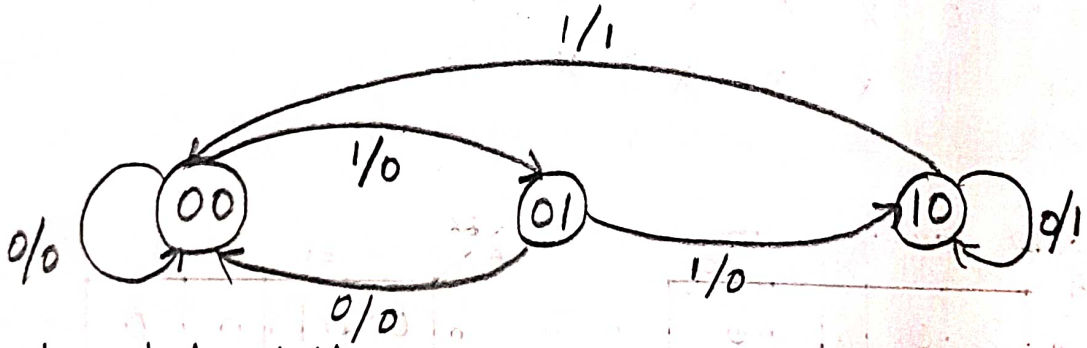
5)



write state table:

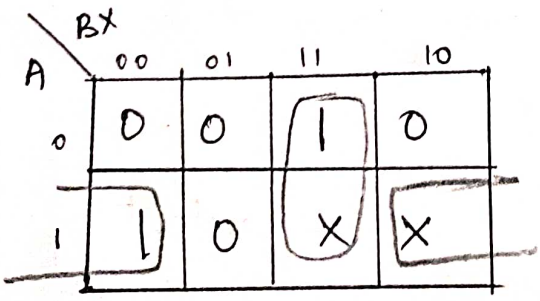
Present state		Next state				output	
A	B	x=0		x=1		x=0	x=1
		A	B	A	B	A	B
0	0	0	0	0	1	0	0
0	1	0	0	1	0	0	0
1	0	1	0	0	0	1	1

Write excitation table of D

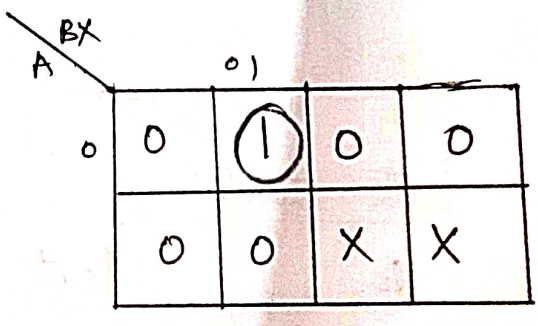
Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

Step 3: write transition table:

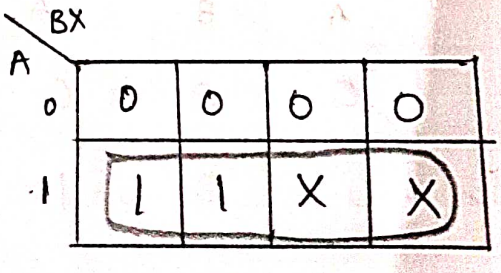
Present			Next		output		
A	B	X	A	B	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	1	0	1	0	1
1	0	1	0	0	0	0	1
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

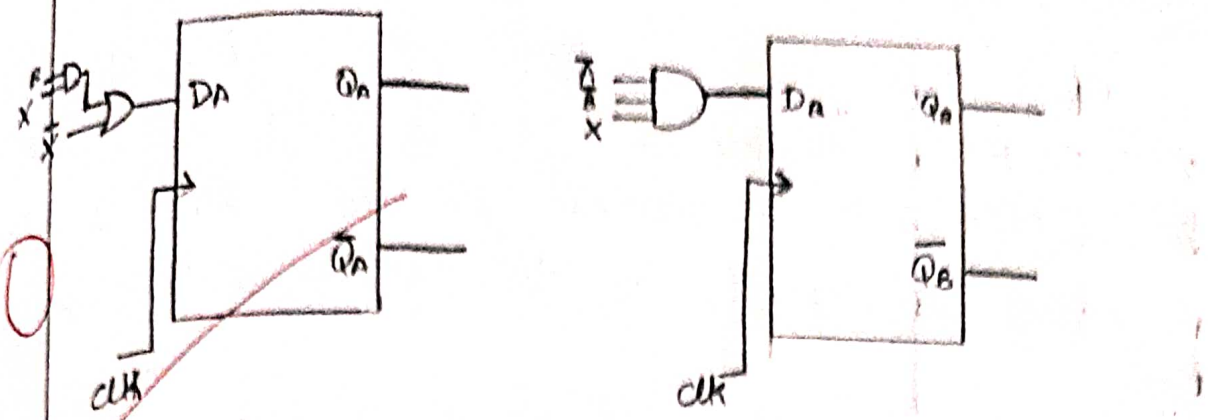


$D_A = BX + \bar{X}$



$D_B = \bar{A}\bar{B}X$





2) Write short notes on EPROM, flash memory & different types of RAM and ROM.

→ EPROM:
(Erasable Programming Read only memory).

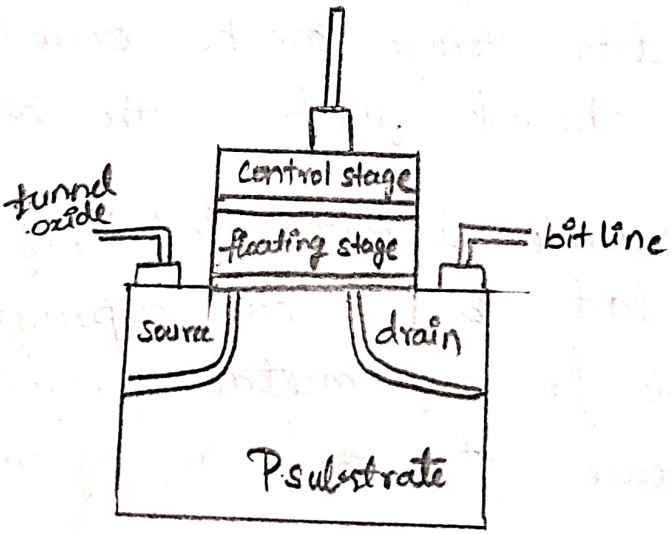
EPROM uses a mos circuitry. It stores a 1's or 0's in packet of charge in the Ic chip layer. It is used by EPROM programmer. The special effect in EPROM is the data storage can be erased by exposing it to UV light through quartz in the chip for 15–20 minutes.

The data erasable is not selected, If erased the entire data is last. but it can reprogrammed. It offically suitable for experimental project, college laboratics because it reprogram data many times over.

Flash memory:

Flash memory is a type of read write memories. It is possible to read a single cell, but while writing it is possible for entire block of cells. Flash memory is depend on transistor with trapped charge.

The floating stage works in presence & absence of charge. In absence of charge it works like the normal mosfet. If +ve charge in control stage it makes a channel between drain and source and current passes. If floating stage is negative it shields the charge somewhat from control stage. and create a P-substrate between source and drain.



RAM (Random access memory).

→ i) Static RAM.

ii) Dynamic RAM

ROM (Read only memory).

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i) PROM (Programming Read only memory)

ii) EPROM (Erasable Programming read only memory.