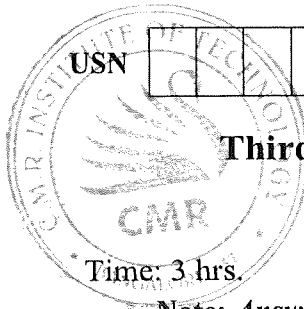


# CBCS SCHEME

17CS32



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## Third Semester B.E. Degree Examination, Feb./Mar. 2022 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- Explain the working of N-channel DE-MOSFET, with the help of neat diagram. (08 Marks)
  - Mention the differences between JFET and MOSFET. (06 Marks)
  - List and explain any one application of FET and its working with neat circuit diagram. (06 Marks)

OR

- What is Multivibrator? Explain the working of Astable multivibrator using 555 timer IC. (08 Marks)
  - Explain the Performance parameters of op-amp. (08 Marks)
  - Figure below shows Fig Q2(c) a biasing configuration using DE-MOSFET. Given that the saturation drain current is 8mA and the pinch off voltage is  $-2V$ . Determine the value of  $V_{GS}$ ,  $I_D$  and  $V_{DS}$ .

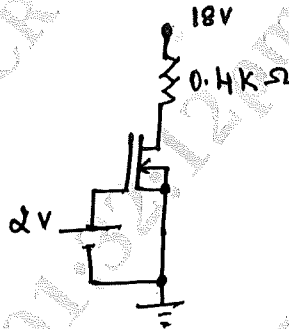


Fig Q2(c)

(04 Marks)

### Module-2

- What are Hazards? Explain the types of Hazards and its covers. (08 Marks)
  - Find the minimal sum and minimal product for the following Boolean function using K-map,  $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13, 14) + \sum d(1, 4, 5, 11)$ . (08 Marks)
  - What is HDL? Write the verilog code for given expression  $Y = AB + \overline{AB}$  using data flow model and behavioural model. (04 Marks)

OR

- Using Quine-McClusky method simplify the following Boolean equation:  
 $f(a, b, c, d) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ . (08 Marks)
  - Design a four input system, in which input system indicates when members divisible by 3 or 5 occur. Find the followings:
    - Write truth table and Boolean expression in  $\Sigma$  and  $\pi$  - notations
    - Using K-map simplify the Boolean expression in minterm form
    - Implement logic circuit using basic gates. (08 Marks)
  - Describe positive and negative logic. (04 Marks)

**Module-3**

- 5 a. Show how using 3 to 8 decoder and multi input OR gates, following Boolean expressions can be realized simultaneously.  
 $F_1(a, b, c) = \sum m(0, 4, 6)$ ,  $F_2(a, b, c) = \sum m(1, 3, 7)$ ,  $F_3(a, b, c) = \sum m(1, 2, 3, 7)$ . (06 Marks)
- b. What is Multiplexer? Implement the following function using 8:1 multiplexer.  
 $f(a, b, c, d) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$  (06 Marks)
- c. Design 7-segment decoder using PLA. (08 Marks)

**OR**

- 6 a. What is magnitude comparator? Explain 2-bit comparator. (08 Marks)
- b. Explain with neat circuit, 3-bit parity generator and 4-bit parity checker for odd parity. (08 Marks)
- c. Show how two 1 to 16 deMUX can be connected to get 1 to 32 deMUX. (04 Marks)

**Module-4**

- 7 a. What is switch contact bounce? Explain the working principle of a simple RS Latch debounce circuit. (08 Marks)
- b. What is Race around condition? With block diagram and truth table, explain the working of JK master slave flip flop. (08 Marks)
- c. Differentiate between Synchronous and Asynchronous counter. (04 Marks)

**OR**

- 8 a. Obtain the state transition diagram and excitation table for SR, D, T and JK flip flops. (08 Marks)
- b. Design a 4-bit SISO register using D-Flip-Flops and explain the working with neat timing diagram. (06 Marks)
- c. Design a synchronous mod – 5 down counter using JK flip-flops. (06 Marks)

**Module-5**

- 9 a. Define Counter. Design a Synchronous counter for the sequence  $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$  using JK flip-flop. (08 Marks)
- b. With a neat block diagram, illustrate the working of digital clock. (06 Marks)
- c. Explain counter type A/D converter. (06 Marks)

**OR**

- 10 a. Explain with block diagram, the operation of successive approximation converter. (08 Marks)
- b. Illustrate the working of dual slope converter with neat diagram (08 Marks)
- c. Explain the terms Accuracy and Resolution for D/A converter. (04 Marks)

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