CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Convert the following Boolean function into their proper canonical form:
(i) $f = \bar{a}\,b + \bar{b}\,c$ (ii) $f(x,y,z) = (x+y)(y+z)$ **(08 Marks)**

b. Simplify the following function using K-map:
i) $f(w,x,y,z) = \sum m(1,3,7,11,15) + \sum d(0,2,4)$
ii) $f(a,b,c,d) = \sum m(0,2,4,5,6,7,8,10,13,15)$ **(12 Marks)**

OR

2 a. Define combinational logic, canonical SOP, canonical POS and PI, with examples. **(08 Marks)**

b. Simplify using Q-M method $y = f(w,x,y,z) = \sum m(0,2,8,10)$. Verify the answer with K- map. **(12 Marks)**

Module-2

3 a. What are Multiplexers? Implement the following using 8:1 multiplexers.
$f(a,b,c,d) = \sum m(2,3,5,6,7)$ **(08 Marks)**

b. Design 2-bit comparator circuit, truth table, K-map and logic circuit. **(12 Marks)**

OR

4 a. Explain the carry look ahead adder. **(10 Marks)**

b. Design 16:1 multiplexer using 8:1 mux. **(05 Marks)**

c. Write a short note on encoders. **(05 Marks)**

Module-3

5 a. Explain the working of Master-Slave JK flip-flop with functional table and timing diagram. **(10 Marks)**

b. Explain working of 3-bit binary ripple counter with the logic and timing diagram. **(10 Marks)**

OR

6 a. Explain the 4 modes of operation of universal shift register with suitable logic diagram. **(10 Marks)**

b. Design mod-6 synchronous counter using JK-flipflop. **(10 Marks)**

Module-4

7 a. With the help of block diagram, explain Mealy and Moore model. **(08 Marks)**

b. Design a sequential circuit using D flip-flop. [Refer Fig.Q7(b)].

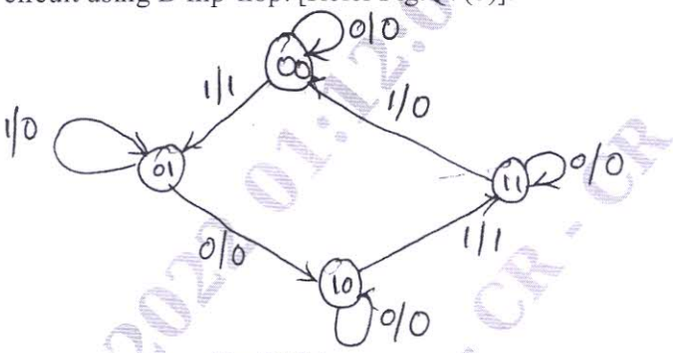

Fig.Q7(b) **(12 Marks)**

OR

8 a. Write procedure for design of clocked synchronous sequential circuit. **(08 Marks)**

b. Analyse the following sequential circuit and draw the state diagram. [Refer Fig.Q8(b)]

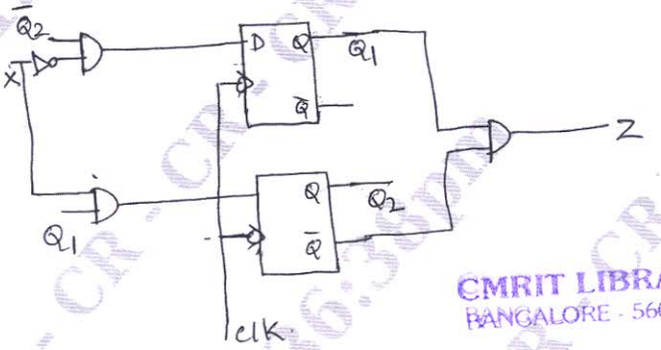

Fig.Q8(b) **(12 Marks)**

Module-5

9 a. Explain briefly history of HDL and structure of HDL. **(10 Marks)**

b. List the classification of VHDL data types and explain with examples. **(10 Marks)**

OR

10 a. Mention styles/types of HDL description. Explain behavioral type with Fulladder example in both VHDL and varilog. **(12 Marks)**

b. Explain varilog data types. **(08 Marks)**

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