CBCS SCHEME

USN | | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define and explain the combinational logic circuit along with block diagram. **(06 Marks)**

b. Develop the canonical minterm and maxterm forms in decimal notation for the following Boolean functions:

i) $X = f(a, b, c, d) = \bar{a}\bar{b} + c\bar{d}$

ii) $Y = f(a, b, c) = (\bar{a} + b)(b + \bar{c})$ **(08 Marks)**

c. Simplify the following function using K-map method and also construct logic circuit for the simplified equation (function).

$Y = f(a, b, c, d) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13, 14)$. **(06 Marks)**

OR

2 a. Simplify the following Boolean function by using Q-M method:

$X = f(a, b, c) = \sum(0, 1, 2, 3, 4, 5, 6)$. **(10 Marks)**

b. Design a combinational logic circuit for valid single digit BCD data, the output is 1 whenever a number is greater than 5 appears at the input. **(05 Marks)**

c. Identify the PI and EPI for the following function:

$M = f(a, b, c, d) = \sum(1, 2, 3, 5, 7, 11, 12, 13, 14, 15)$. **(05 Marks)**

Module-2

3 a. Draw and explain the circuit for 3 to 8 decoder. **(06 Marks)**

b. Design and implement a full adder circuit using logic gates. **(08 Marks)**

c. Write a short notes on PLD's and FPGA. **(06 Marks)**

OR

4 a. Define MUX and explain 4:1 MUX with the help of logic diagram using gates. **(06 Marks)**

b. Explain 4-bit carry look-ahead adder with diagram. **(08 Marks)**

c. Design and implement 1-bit comparator circuit. **(06 Marks)**

Module-3

5 a. Compare sequential circuit and combinational circuits. **(06 Marks)**

b. Write a short notes on SR-latch. **(06 Marks)**

c. Illustrate master-slave J-K flip-flop using NAND Gates. **(08 Marks)**

OR

6 a. Distinguish between synchronous and asynchronous counter. **(06 Marks)**

b. Explain 4-bit universal shift register along with diagram. **(08 Marks)**

c. Explain the working of clocked SR-FF using NAND Gates. **(06 Marks)**

Module-4

7 a. Explain Mealy and Moore model with diagrams. **(10 Marks)**

b. Design and develop Mod-6 synchronous counter using T-FF. **(10 Marks)**

OR

8 a. Construct the excitation table, transition table, state table and state diagram for the following sequential circuit. (Refer Fig.Q.8(a)). **(14 Marks)**

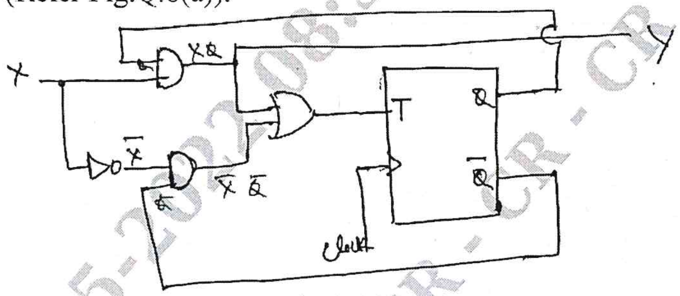

Fig.Q.8(a)

b. List out the applications of shift registers along with brief explanation. **(06 Marks)**

Module-5

9 a. Explain the operation of serial adder with accumulator. **(12 Marks)**

b. Illustrate state assignment rules. **(08 Marks)**

OR

10 a. Write a short notes on:

i) Sequential circuit design steps

ii) BCD to Ex-3 code convertor. **(10 Marks)**

b. Explain 4-bit Ring and Johnson counter along with diagram. **(10 Marks)**

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