CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Obtain the expressions for Z_i, Z_0 and A_v for fixed bias transistor circuit using r_e model. **(10 Marks)**

b. What is Darlington Connection? Calculate the DC bias voltage and currents in the Darlington emitter follower circuit given.

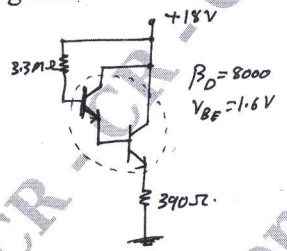

Fig.Q1(b) **(05 Marks)**

c. For a fixed bias circuit with $R_B = 330K\Omega$, $R_C = 2.7K\Omega$ and $V_{CC} = 8V$. Find Z_i, Z_o and A_V if transistor used has $h_{fe} = 120$, $h_{ie} = 1.175K\Omega$ and $h_{oe} = 20\mu A/v$. **(05 Marks)**

OR

2 a. Obtain expression for Z_i, Z_0 and A_V for Emitter follower circuit (CC – configuration of transistor) with $r_0 = \infty$. **(10 Marks)**

b. For the voltage divider bias circuit with $R_1 = 56K\Omega$, $R_2 = 8.2K\Omega$, $R_C = 6.8K\Omega$, $R_E = 1.5K\Omega$. Find : Z_i, Z_0 and A_V if transistor used has $h_{fe} = 120$, $h_{ie} = 1.175K\Omega$ and $h_{oe} = 20\mu A/v$. **(06 Marks)**

c. Draw and explain Hybrid – II model of transistor in CE configuration. **(04 Marks)**

Module-2

3 a. Explain the construction and working of N-channel JFET. Also explain the drain the transfer characteristics of JFET with neat diagrams. **(10 Marks)**

b. The fixed bias configuration shown in Fig.Q3(b), has $V_{GSQ} = -2V$, $I_{DSS} = 10mA$, $I_{DQ} = 5.6mA$, $V_P = -8V$, $Y_{os} = 40\mu s$. Find Q_m, r_d, Z_i, Z_0 and A_V.

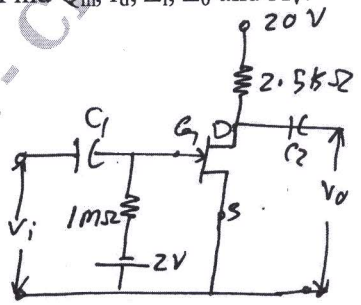

Fig.Q3(b) **(05 Marks)**

c. With necessary equivalent circuit obtain the expression for Z_i, Z_0 and A_V for self Bias configuration with Bypass capacitor of JFET. **(05 Marks)**

OR

4 a. With necessary equivalent circuit obtain the expression for Z_i, Z_0 and A_V for a JFET common gate configuration. **(10 Marks)**

b. Find Z_i, Z_0 and output voltage if $g_m = 2.6mS$ of both stages.

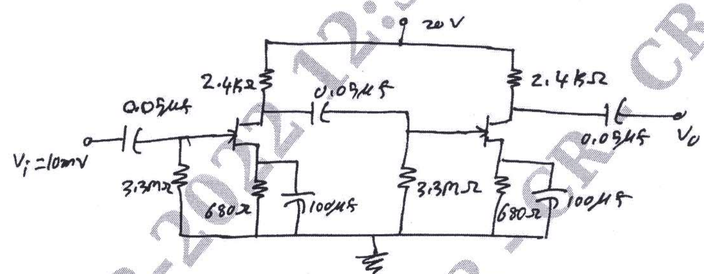

Fig.Q4(b) **(06 Marks)**

c. Identify the differences between enhancement and repletion MOSFET (any two). **(04 Marks)**

Module-3

5 a. What is Miller effect? Derive expression for Miller capacitance for an amplifier. **(08 Marks)**

b. Determine $f_{L_G}, f_{L_C}, f_{L_S}, f_{H_i}$ and f_{H_o} for the given FET amplifier circuit with

$C_{W_i} = 5pf$, $C_{W_o} = 6pf$, $C_G = 0.01\mu f$, $C_C = 0.5\mu f$, $C_S = 2\mu f$,

$I_{DSS} = 8mA$, $V_P = -4V$, $r_d = \infty$, $V_{DD} = 20V$, $V_{GS} = -2V$

$C_{gd} = 2pf$, $C_{gs} = 4pf$, $C_{ds} = 0.5pf$.

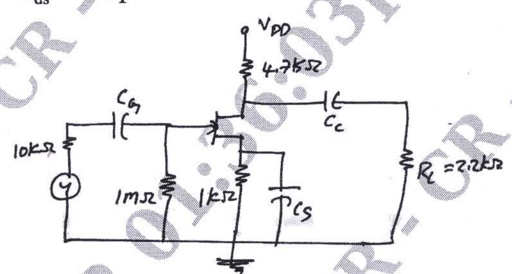

Fig.Q5(b) **(12 Marks)**

OR

6 a. Derive the expressions for low frequency cut-offs for a voltage divider transistor with R_S and R_L. **(08 Marks)**

b. The input power to a device is 10000W at a voltage of 1000V. The output power is 500W and the output impedance is 20Ω. Find : i) power gain in dB ii) voltage gain in dB. **(04 Marks)**

c. For the given circuit of transistor amplifier find f_{β_1}, f_{H_i} and f_{H_0}.

Given $r_0 = \infty$, $C_{be} = 36pf$, $C_{bc} = 4pf$, $C_{ce} = 1pf$, $C_{Wi} = 6p$, $C_{wo} = 8pf$, and $r_e = 15.76\Omega$.

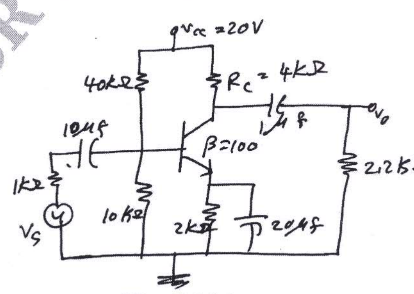

Fig.Q6(c) **(08 Marks)**

Module-4

7 a. Derive expressions for voltage gain, Z_{if} and Z_{of} of voltage series feedback amplifier with necessary feedback connections. **(08 Marks)**

b. With neat diagram and necessary expressions explain tuned Hartely Oscillators. Using transistor. **(06 Marks)**

c. Describe the working of series crystal oscillator. **(06 Marks)**

OR

8 a. For a practical current series feedback circuit drive expression for A_{Vf}, Z_{If} and Z_{Of}. **(08 Marks)**

b. With neat diagram and necessary expressions explain :
i) Wien bridge Oscillator
ii) UJT Oscillator. **(12 Marks)**

Module-5

9 a. Calculate the efficiency of a transformer coupled class A amplifier for supply of 12V and output of $V_p = 6V$. **(05 Marks)**

b. With neat diagram explain the working of transformer – coupled push – pull amplifier. **(08 Marks)**

c. Describe with block diagram the series type of voltage regulator. **(07 Marks)**

OR

10 a. Calculate the output voltage and the Zener current in the regulator circuit given for $R_L = 1k\Omega$.
$R = 220\Omega$, $V_z = 12V$, $\beta = 50$.

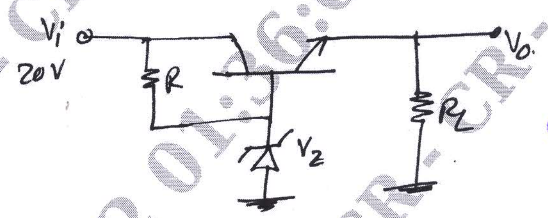

Fig.Q10(a) **(05 Marks)**

b. Explain the working of class D amplifier with block diagram and necessary waveforms. **(07 Marks)**

c. With necessary circuit diagram and characteristics curve, show that the maximum efficiency of a series fed class A amplifier is 25%. **(08 Marks)**

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