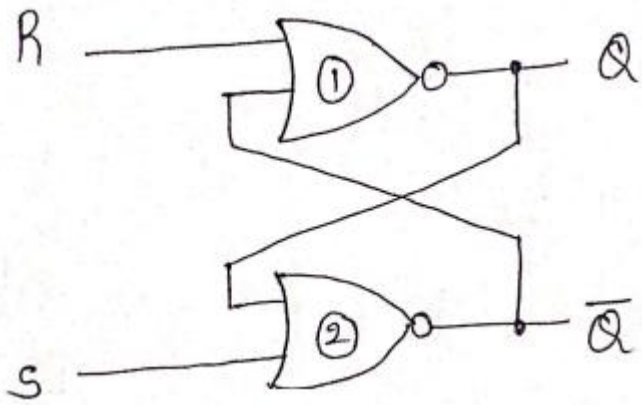
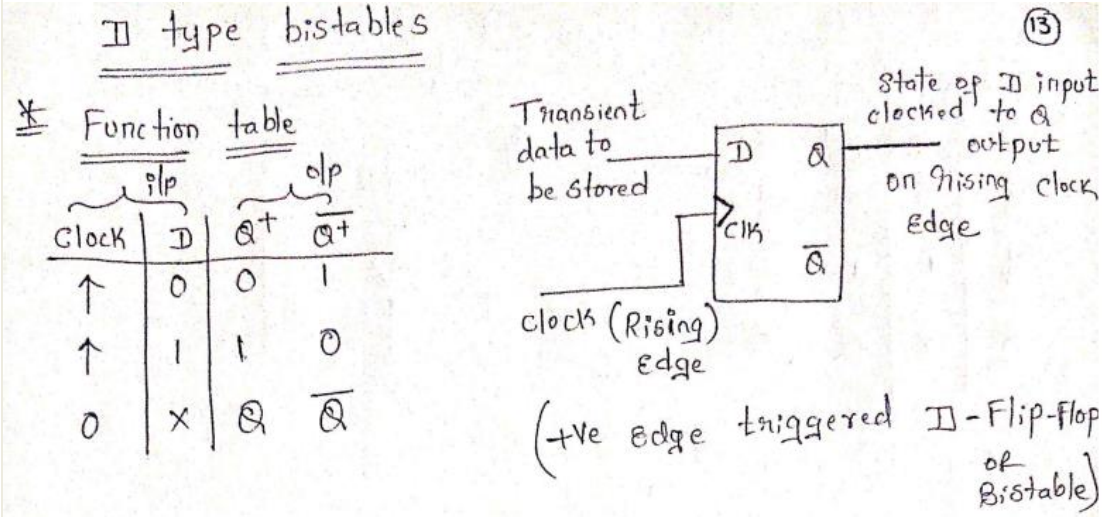
CMR INSTITUTE OF TECHNOLOGY

ROLL NO. | | | | | |

Internal Assessment Test - I

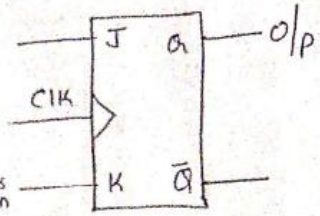
Sub:	**Basic Electronics**							Code:	**21ELN14**
Date:	25-01-2022	Duration:	90 mins	Max Marks:	50	Sem:	I	Sec:	I,J,K,L,M,N, O
Answer Any FIVE FULL Questions									

		Marks	OBE CO	OBE RBT
1.	Explain the following logic gates with their symbols, truth table. a. XOR Gate b. AND Gate c. OR Gate d. NAND Gate. NOR Gate **2 MARKS FOR EACH SYMBOL, TRUTH TABLE, OPERATION**	[10]	CO2	L1
2.a	Define bistable circuits. Explain R-S bistable using NOR gates. Mention one disadvantage of R-S bistable. **CIRCUIT 1 MARKS** **DEFINITION 1 MARKS** **OPERATIONS 3 MARKS** **DISADVANTAGE 1 MARKS** 	[06]	CO2	L2
2.b	Write the logic symbol and truth table of D and JK bistable. **2 MARKS FOR EACH TABLE** 	[04]	CO2	L2

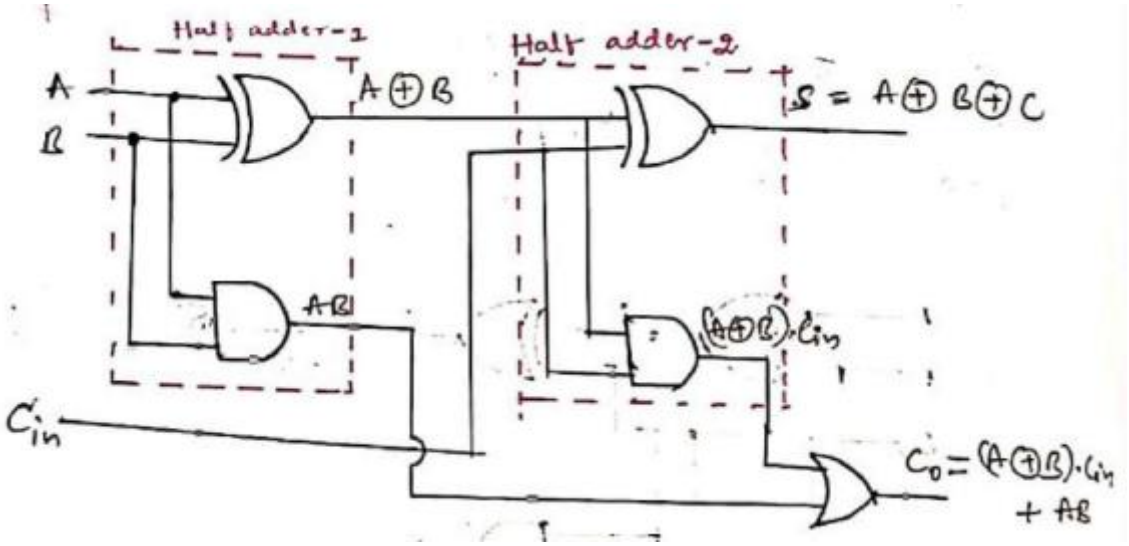
* Positive edge triggered JK-Flip Flop | JK-bistable (14)

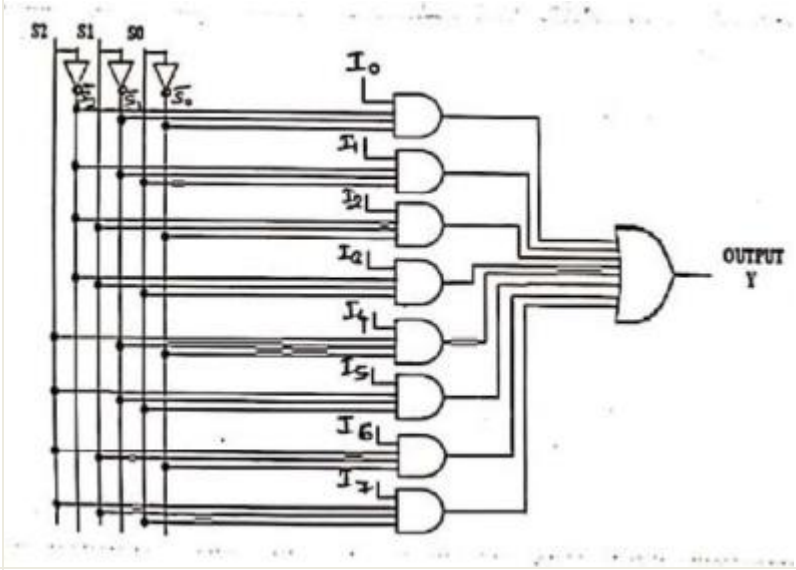
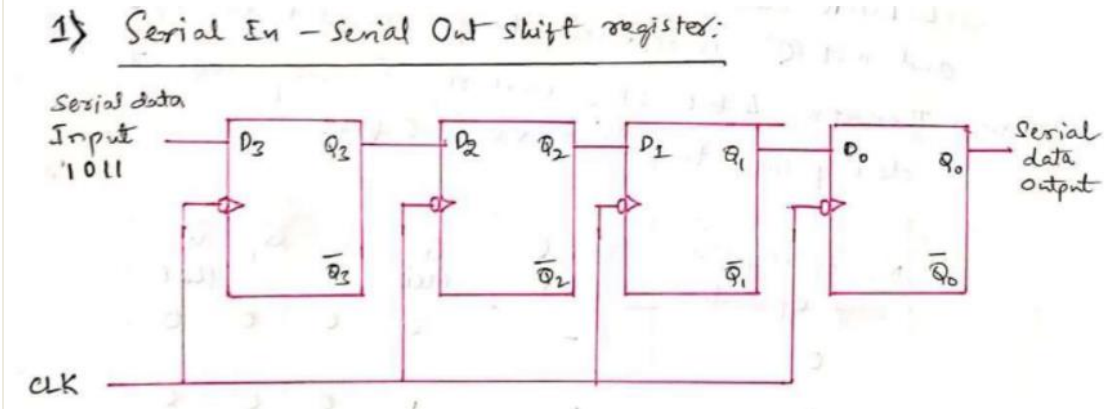
Function table

Clk	J	K	Q^+	$\bar{Q}^+$	Comment
↑	0	0	Q	$\bar{Q}$	No change in state of the Q output on next clock transition
↑	0	1	0	1	Q=0, on next clock transition
↑	1	0	1	0	Q=1, on next clock transition
↑	1	1	$\bar{Q}$	Q	Q output changes to the opposite state on the next clock transition
0	x	x	Q	$\bar{Q}$	No change in o/p



3.	Perform the following Conversions. **2 MARKS FOR EACH** (i) $(1011011)_2 \rightarrow (?)_{16}$ (ii) $(1234.56)_{16} \rightarrow (?)_2$ (iii) $(101110100.1101)2 \rightarrow (?)_{16}$ (iv) $(ABCD.EF)_{16} \rightarrow (?)_2$ (v) $(988.86)_{16} \rightarrow (?)_2$	[10]	CO2	L2
4	Realize a full adder circuit using two half adder and a OR gate, with truth table and logic expressions. **CIRCUIT – 3 MARKS , EXPLAINATION- 3 MARKS, TRUTH TABLE AND BOOLEAN SIMPLIFICATION- 4 MARKS**	[10]	CO2	L3

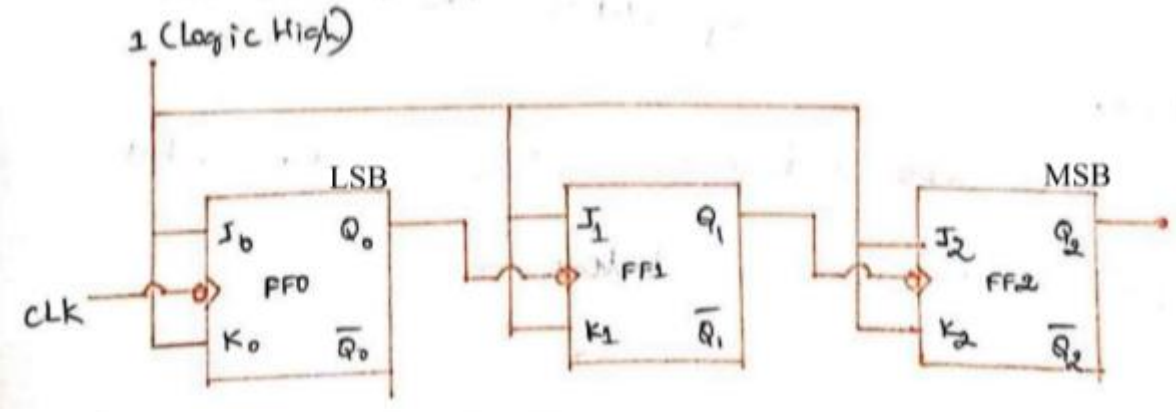


5.	With neat circuit diagram explain the operation of 8:1 Multiplexer. **CIRCUIT – 3 MARKS , EXPLAINATION- 3 MARKS, TRUTH TABLE AND BOOLEAN EXPRESSION- 4 MARKS** 	[10]	CO2	L2
6.	What is a shift register? Explain the working of SISO shift register with neat diagram and waveforms. **DEFINITION- 1, CIRCUIT – 2 MARKS , EXPLAINATION- 3 MARKS, OPERATION TABLE AND WAVEFORM- 4 MARKS** 	[10]	CO2	L3

No. of Negative edge of clock	Serial input	Q_3 (MSB)	Q_2	Q_1	Q_0 (LSB)
0	–	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	0	0	1	1	0
4	1	1	0	1	1
5	–	–	1	0	1
6	–	–	–	1	0
7	–	–	–	–	1

7.	Explain the operation 3-bit ripple UP counter with relevant diagram and waveforms.	[10]	CO2	L4

CIRCUIT – 2 MARKS, EXPLAINATION- 4 MARKS, OPERATION TABLE AND WAVEFORM- 4 MARKS



Truth table of 3-bit Ripple counter.

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1