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Internal Assessment Test 4– March 2022

Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch	ISE	
Date:	21/03/2022	Duration:	3 Hrs	Max Marks:	100	Sem/Sec:	III / A, B and C		OBE	

Answer any FIVE FULL Questions

			MARKS	CO	RBT
		Module 1,5			
1	a	With a neat circuit diagram and mathematical analysis explain voltage divider bias circuit by approximate analysis	10	CO1	L2
	b	Explain the construction, working and characteristics of photodiode.	10	CO1	L2
		or			
2	a	Explain Analog to Digital and Digital to Analog converter with an example.	10	CO2	L2
	b	Write a note on Ring counter and Johnson counter.	10	CO4	L2
		Module 1,2			
3	a	Explain current to voltage converter and adjustable voltage regulator.	10	CO1	L2
	b	Solve S=F (A, B, C, D) = Σm (2,3,4,5,13,15) + Πd (8, 9, 10, 11) using MEV to get minimum SOP expression.	10	CO3	L3
		or			
4	a	With neat sketch, explain the working principle of SISO shift register.	10	CO4	L2
	b	With the help of state graph, state transition tables and timing diagram explain sequential parity checker.	10	CO4	L2
		Module 5			
5	a	Solve S= F (A, B, C, D) = Σm (0,1,4,8,9,10) + d (2,11) using K map to get minimum SOP expression.	10	CO3	L3
	b	Find the minimum SOP for the function f (a, b, c, d) =∑m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14) using Quine-McCluskey method. Determine prime implicants.	10	CO3	L3
		or			
6	a	With a block diagram explain the working of 4-bit parallel adder with accumulator.	10	CO4	L2
	b	Design mod 5 counter using JK flip flops	10	CO4	L3
		Module 1,5			
7	a	With a neat diagram and waveform, explain the working principle of astable multi vibrator using IC 555 timer.	10	CO1	L2
	b	Explain how 4 bits register with data, load, clear and clock input is constructed using D flip flops.	10	CO4	L2
		or			
8	a	Design 3-bit synchronous binary counter using transition table of T flip flop.	10	CO4	L3
	b	Using a 741 op-amp with a supply of 12V, design inverting Schmitt trigger circuit to have trigger points of ±2V	10	CO1	L3
		Module 1,5			
9	a	With hysteresis characteristics explain the working of Inverting Schmitt Trigger circuit.	10	CO1	L2
	b	Construct a 2nd order high pass filter with neat sketch and write its response curve	10	CO1	L3
		or			
10	a	Design a random counter using T FF whose transition is $0 \rightarrow 4 \rightarrow 7 \rightarrow 2 \rightarrow 3 \rightarrow 0$	10	CO4	L3
	b	With an example explain Petrik's method.	10	CO3	L2

Faculty Signature CCI Signature HOD Signature

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Internal Assessment Test 4 – March 2022

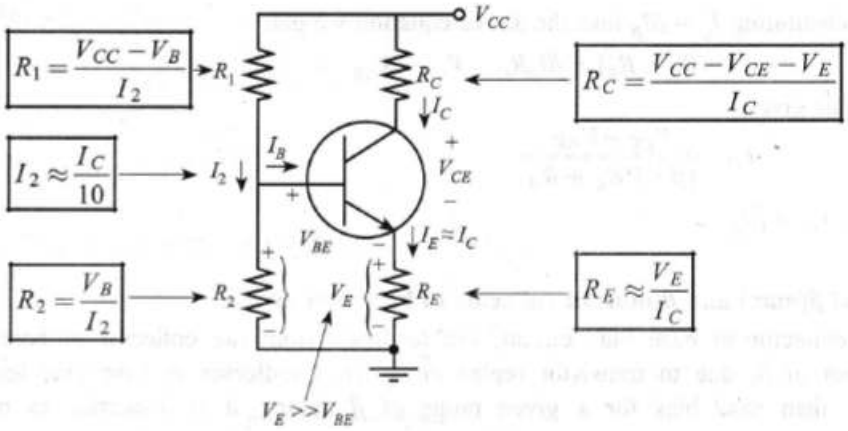
Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	ISE	
Date:	21/3/2022	Duration:	180 min's	Max Marks:	100	Sem/Sec:	III / A, B and C			OBE

Answer any FIVE FULL Questions

		MARKS	CO	RBT
1	a. With a neat circuit diagram and mathematical analysis explain voltage divider bias circuit by approximate analysis	10	CO1	L2

Solution:

Voltage divider bias is the most stable of the three basic transistor biasing circuits. A voltage divider circuit is shown in the following Figure.



There is an emitter resistor R_E connected in series with Emitter terminal, so that the total dc load in series with the transistor is ($R_C + R_E$). Resistors R_1 and R_2 constitutes a voltage V_B.

Applying KVL to the loop V_{CC}, R_1, and R_2, we get;

$V_{CC} - I_1R_1 - I_2R_2 = 0$ Or, $I_1R_1 + I_2R_2 = V_{CC}$ ---------- (5)

We have; $I_1 = I_2 + I_B$

Voltage divider bias circuits are normally designed to have a voltage divider current I_2 very much greater than transistor base current I_B. i.e., $I_2 >> I_B$. Hence, $I_1 \approx I_2$ ---------- (6)

Using 6 in 5; $I_2R_1 + I_2R_2 = V_{CC}$ *i.e.*, $I_2(R_1 + R_2) = V_{CC}$ Or, $\boldsymbol{I_2 = (V_{CC}) / (R_1 + R_2)}$

V_B is the voltage across R_2. i.e., $V_B = I_2R_2$ Or, $\boldsymbol{V_B = (V_{CC} * R_2) / (R_1 + R_2)}$

V_E is the voltage across R_E. i.e., $\boldsymbol{V_E = I_ER_E}$

Applying KVL to the base-emitter loop; $V_B - V_{BE} - V_E = 0$ i.e., $\mathbf{V_{BE} = V_B - V_E}$

Or, $V_E = V_B - V_{BE}$ i.e., $I_ER_E = V_B - V_{BE}$ Hence, $\boldsymbol{I_E = (V_B - V_{BE}) / R_E}$

Applying KVL to the collector-emitter loop; $V_{CC} - I_CR_C - V_{CE} - I_CR_E = 0$ $[I_E \approx I_C]$

i.e., $\boldsymbol{V_{CE} = V_{CC} - I_C(R_C + R_E)}$

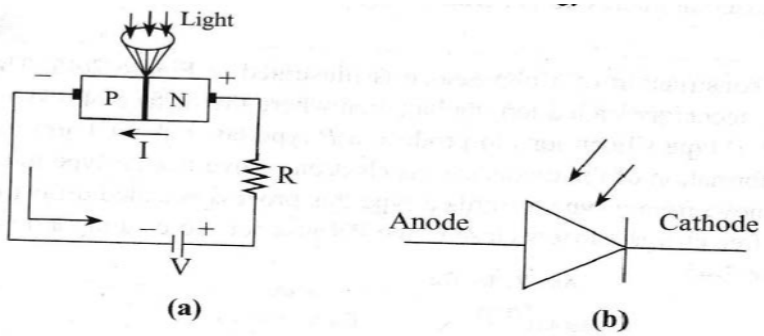
	b. Explain the construction, working and characteristics of photodiode	10	CO1	L2

Solution:

Working Principle:

When the conventional diode is reverse biased, the depletion region starts expanding and the current starts flowing due to minority charge carriers. With the increase of reverse voltage, the reverse current also starts increasing. The same condition can be obtained in photodiode without applying reverse voltage.

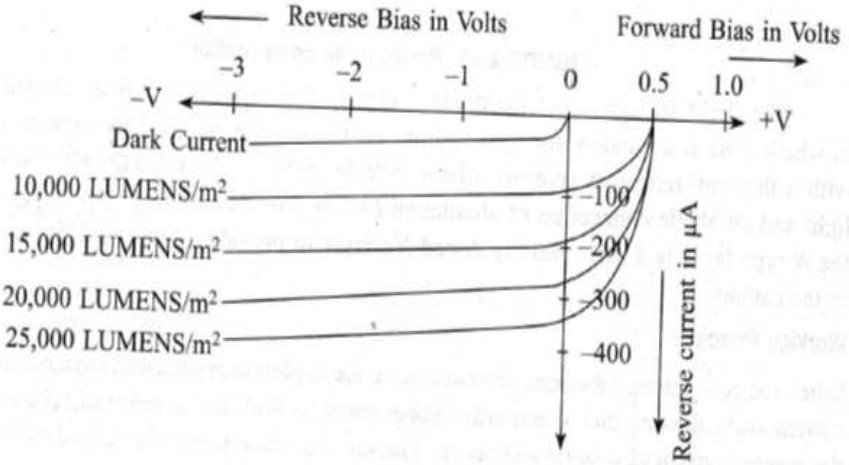
The following Figure shows photo diode bias symbol. The junction of Photodiode is illuminated by the light source; the photons strike the junction surface. The photons impart their energy in the form of light to the junction. Due to which electrons from valence band get the energy to jump into the conduction band. This leaves positively charged holes in the valence band, so producing 'electron-hole pairs' in the depletion layer. Some electron-hole pairs are also produced in P and N layers, but apart from those produced in the diffusion region N layers, most will be re-absorbed within the P and N materials as heat. The electrons in the depletion layer are then swept towards the positive potential on the cathode, and the holes swept towards the negative potential on the anode, so creating a photo current. In this way, the photodiode converts light energy into electrical energy.



(a) (b)

V-I Characteristics of Photodiode:

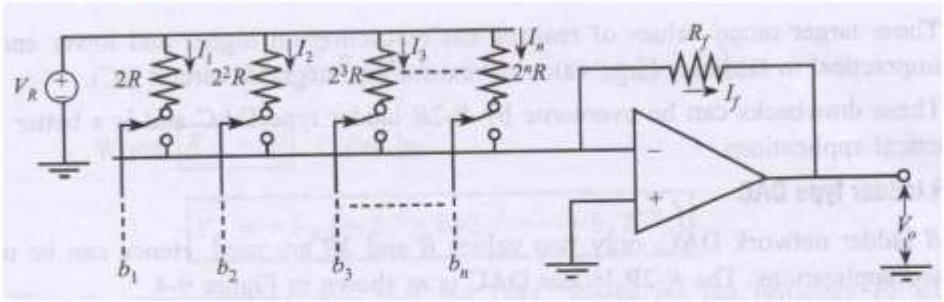
The characteristics curve of the photodiode can be understood with the help of the following Figure. The characteristics are shown in the negative region because the photodiode can be operated in reverse biased mode only.



2	a. Explain Analog to Digital and Digital to Analog converter with an example **Solution:**	10	CO2	L2

Binary Weighted Resistor DAC:

The following Figure shows binary weighted resistor DAC circuit using n-electronic switches to control the binary inputs $b_1, b_2, \ldots, b_n$.



When the switch is ON; $I = \frac{V_R}{R}$ When the switch is OFF; I = 0.

Due to very high input impedance of Op-Amp, the toatl current I will flow through R_f. The total current trough R_f is; $I = I_1 + I_2 + I_3 + \ldots + I_n$

$$= \frac{V_R}{2^1R}b_1 + \frac{V_R}{2^2R}b_2 + \frac{V_R}{2^3R}b_3 + \ldots + \frac{V_R}{2^nR}b_n$$

$$= \frac{V_R}{R}[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n}]$$

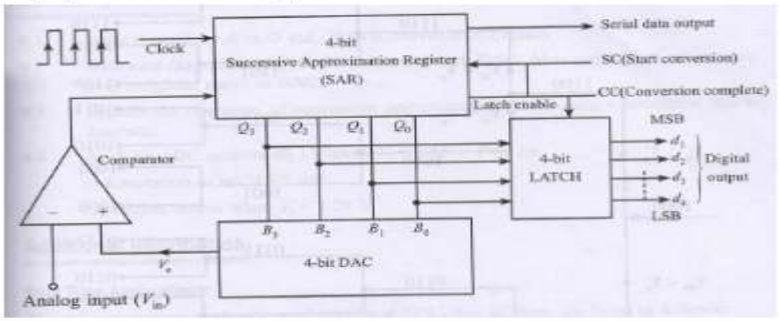
The output voltage is; $V_0 = -I_f R_f$

$$i.e., V_0 = \frac{-V_R}{R} R_f [b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n}]$$

If $R_f = R$; Or, $\boldsymbol{V_0 = -V_R[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n}]}$

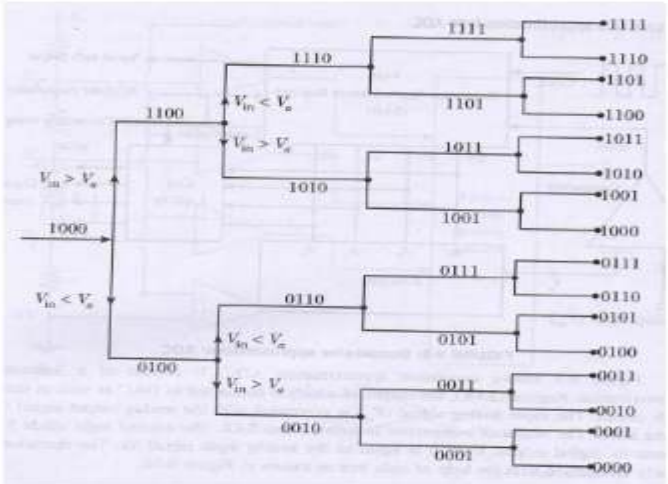
Successive Approximation type ADC:

The following Figure shows successive approximation ADC.



At the start of conversion cycle, start conversion terminal is made high. On the first clock pulse, the output of the SAR is made 1000. The DAC produces an analog voltage (V_a) proportional to 1000. This analog voltage is compared with input analog signal (V_{in}).

If $V_{in} > V_a$ the comparator output will be high and SAR keeps Q3 high. On the other hand, if $V_{in} < V_a$ then the comparator output becomes low and SAR resets Q3 to low. If $V_{in} > V_a$, SAR follows the upward path in code tree and if $V_{in} < V_a$, SAR follows downward path.

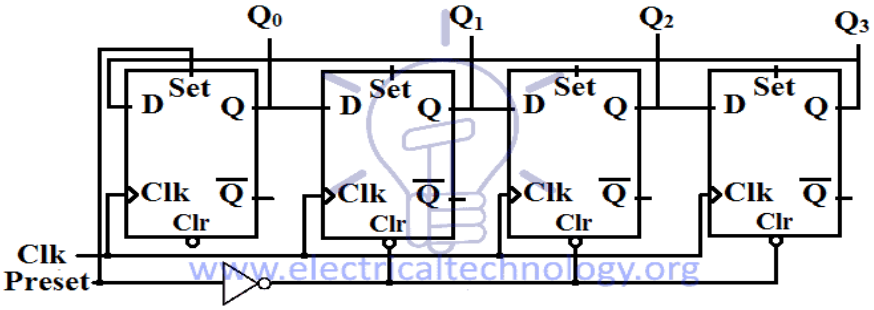


	b. Write a note on Ring counter and Johnson counter.	10	CO1	L2

Solution:

Working of Ring Counter

Ring counter's state needs to be set before the operation. Since ring counter circulates 1 through all stages, and there are no external inputs except the clock signal. So we need to set its state to initial state 1000 manually. We need to set the first stage flip-flop and clear the rest of the stages to obtain the state 1000.The preset input pin is designed to do this function. The schematic of ring counter is given below:



First, we need to set the initial state 1000 through preset input.

Whenever the first clock edge hits the counter the outputs of each stage shifts to the next succeeding stage. And the output of the last will shift to the first stage making the state 0100.

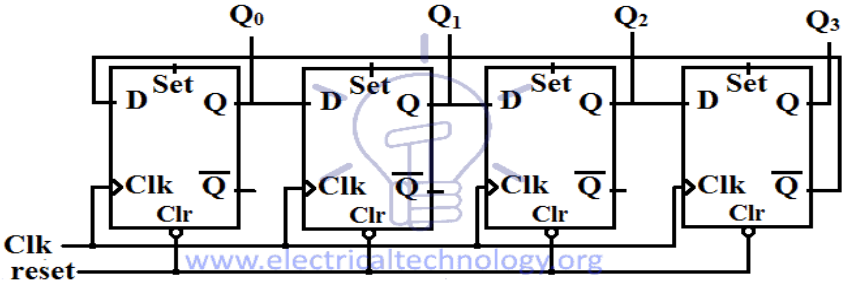
Upon next clock cycle, each stage will update its state according to its input. So the '1' will be shifted to the third stage making the state 0010. Upon another clock cycle, the '1' will reach the last stage making the 0001.

Now upon next clock cycle, '1' from the last stage (flip-flop) will shift back to the first stage making the initial state 1000. And it starts again from the first state repeating itself considering the clock signal is provided. This is how the data inside the ring counter circulates in the ring.

Ring counter divides the frequency of the clock signal by 'n'. n is the bit size of the ring counter. So ring counter can be used as a frequency divider.

Johnson Counter Schematic Design

The schematic of 4-bit Johnson counter consists of 4 D-flip flops or 4 JK-flip flops. These flip-flops are connected with each other in cascade setup. The output of each flip-flop is connected with the input of the succeeding flip-flop. The complemented output of the last flip-flop is connected with the input of the first flip-flop. The Same clock input is connected with all flip-flops. There is clear input for resetting the state to default 0000. Johnson counter's schematic design is given below.



Working of Johnson Counter

The default state of Johnson counter is 0000 thus before starting the clock input we need to clear the counter using clear input.

Whenever a clock edge hits the counter the output of each flip-flop will transfer to the next stage (flip-flop) but the inverted output of the last flip-flop will shift to the first stage making the state 1000.

Upon next clock cycle, another '1' will stack in from the left side as the inverted output of the last stage will be shifted to the first stage.

On next clock cycle, another '1' will add in from left until the state becomes 1111.

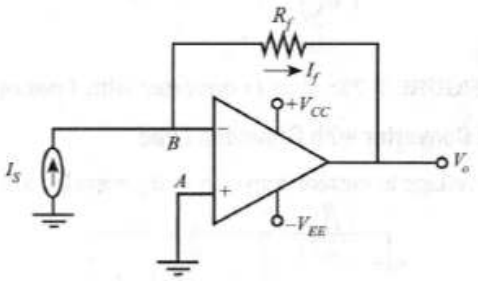
Now that the last flip-flop's output is '1', the next clock cycle will shift the invert of the last flip-flop which is '0' into the first flip-flop. It will result in stacking '0' from the left side. This stacking of the first 0 will make the state 1111 into 0111.

The next coming clock cycles will stack in 0's from the left making the states 0011, 0001 & 0000 with each clock cycle. Eventually, it reaches its default state and it starts from the beginning again.

3	a. Explain current to voltage converter and adjustable voltage regulator. **Solution:**	10	CO1	L2

CURRENT TO VOLTAGE (C TO V) CONVERTER:

Consider the simple Op-Amp circuit to convert I to V, as shown in the following Figure.



Since, current through the Op-Amp is negligible;$I_S = I_f$

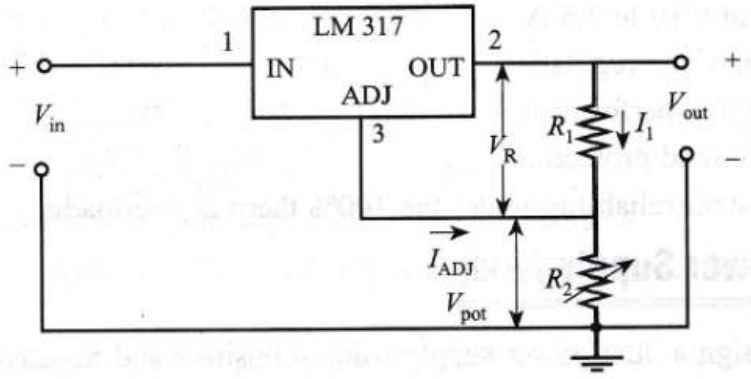
$$I_s = I_f = \frac{V_B - V_0}{R_f}$$

By virtual ground concept; as node A is grounded, node B will be virtually grounded. Therefore, $V_B = 0$. Therefore,

$$I_s = \frac{-V_0}{R_f} \quad Or, \quad V_0 = I_S R$$

Thus, output is proportional to the input current I_S, and the circuit works as I to V converter.

LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 V to 57 V. LM337 is an example of negative adjustable voltage regulator. LM337 is actually a compliment of LM317 which are similar in operation and design with the only difference being polarity of regulated output voltage.



Connection of LM317 Adjustable Voltage Regulator

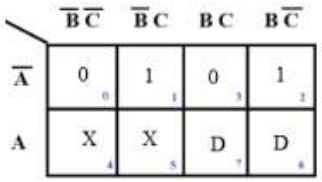
The resistors R_1 and R_2 determine the output voltage V_{out}. The resistor R_2 can be adjusted to get the output voltage in the range of 1.21 V to 57 V. The output voltage is given by;

$$V_{out} = V_R (1 + R_2/R_1) + I_{ADJ} R_2$$

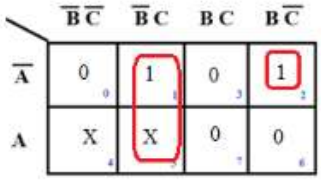
	b. Solve S=F (A, B, C, D) = Σm (2,3,4,5,13,15) + Πd (8, 9, 10, 11) using MEV to get minimum SOP expression. **Solution:**	10	CO3	L3
4	a. With neat sketch, explain the working principle of SISO shift register. **Solution:**	10	CO4	L2

A	B	C	D	Y	MEV
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	1	1
0	0	1	1	1	
0	1	0	0	1	1
0	1	0	1	1	
0	1	1	0	0	0
0	1	1	1	0	
1	0	0	0	X	X
1	0	0	1	X	
1	0	1	0	X	X
1	0	1	1	X	
1	1	0	0	0	D
1	1	0	1	1	
1	1	1	0	0	D
1	1	1	1	1	

SOP: $Y = \overline{B}C + \overline{A}B\overline{C} + AD$

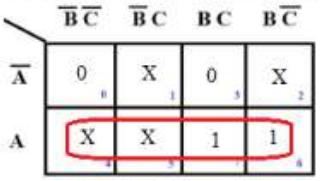


1)Write all the variables as 0 , leave minterms, 0's and don't cares as it is and obtain the SOP expression.



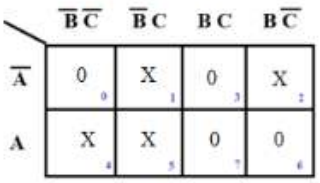
SOP1 : $\overline{B}C$, $\overline{A}B\overline{C}$

2) Replace all occurances of D with 1, all occurrences of D' with 0 and all 1's with don't care. Leave 0's and don't cares as it is



SOP2 : A D

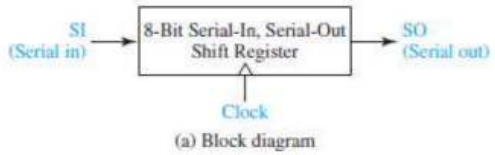
3) Replace all occurrences of D' with 1, all occurrences of D with 0 and all 1's with don't care. Leave 0's and don't cares as it is.



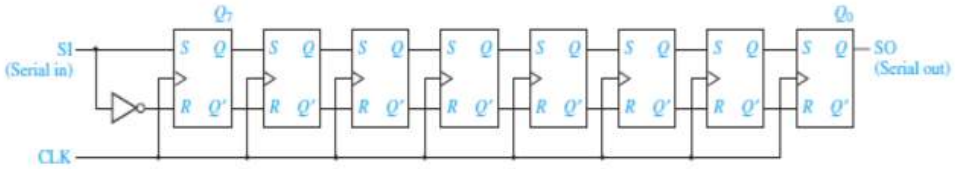
NO SOP

Shift registers with 4, 8, or more flip-flops are available in integrated circuit form. The following Figure illustrates an 8-bit serial-in, serial-out shift register. Serial in means that data is shifted into the first flip-flop one bit at a time, and the flip-flops cannot be loaded in parallel. Serial out means that data can only be read out of the last flip-flop and the outputs from the other flip-flops are not connected to terminals of the integrated circuit.

8-Bit Serial-in, Serial-out Shift Register

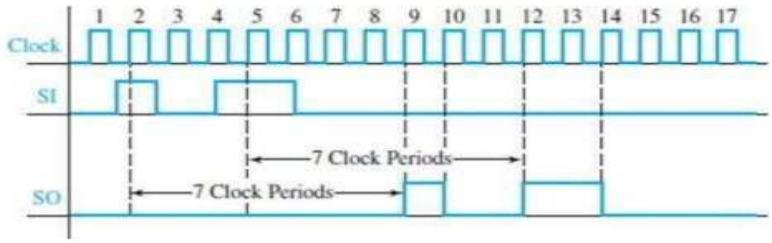


(a) Block diagram



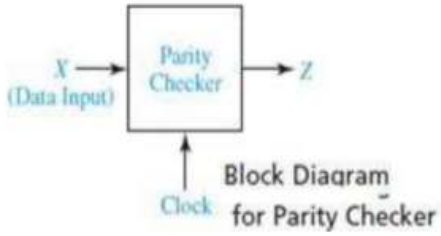
The inputs to the first flip-flop are $S = SI$ and $R = SI'$. Thus, if $SI = 1$, a 1 is shifted into the register when it is clocked, and if $SI = 0$, a 0 is shifted in. The following Figure shows a typical timing diagram.

Typical Timing Diagram for Shift Register

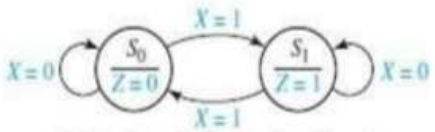


The following Figure (a) shows a 4-bit parallel-in, parallel-out shift register. Parallel-in implies that all four bits can be loaded at the same time, and parallel-out implies that all bits can be read out at the same time. The shift register has two control inputs, shift enable (Sh) and load enable (L). If $Sh = 1$ (and $L = 1$ or $L = 0$), clocking the register causes the serial input (SI) to be shifted into the first flip-flop, while the data in flip-flops Q3,Q2, and Q1 are shifted right. If $Sh = 0$ and $L = 1$, clocking the shift register will

	b. With the help of state graph, state transition tables and timing diagram explain sequential parity checker. **Solution:**	10	CO4	L2
5	a. Solve S= F (A, B, C, D) = Σm (0,1,4,8,9,10) + d (2,11) using K map to get minimum SOP expression **Solution:**	10	CO3	L3



Block Diagram for Parity Checker



State Graph for Parity Checker

The sequential circuit must -*remember*‖ whether the total number of 1 inputs received is even or odd; therefore, only two states are required. We will designate these states as S0 and S1, corresponding respectively to an even number of 1's received and an odd number of 1's received. We will start the circuit in state S0 because initially zero 1's have been received, and zero is an even number.

As indicated in state graph (above Figure), if the circuit is in state S0 (even number of 1's received) and X = 0 is received, the circuit must stay in S0 because the number of 1's received is still even. However, if X = 1 is received, the circuit goes to state S1 because the number of 1's received is then odd.

Similarly, if the circuit is in state S1 (odd number of 1's received) a 0 input causes no state change, but a 1 causes a change to S0 because the number of 1's received is then even.

The output Z should be 1 whenever the circuit is in state S1 (odd number of 1's received). The output is listed below the state on the state graph.

The following Table (a) gives the same information as the state graph in tabular form. The table shows that if the present state is S0, the output is Z = 0, and if the input is X = 1, the next state will be S1.

(a)

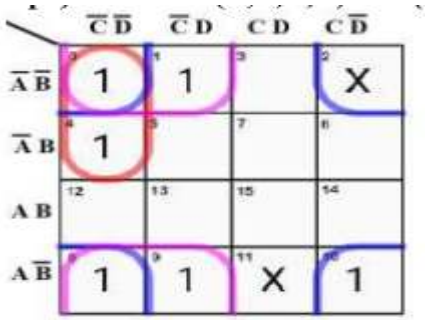
Present State	Next State X = 0	Next State X = 1	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

(b)

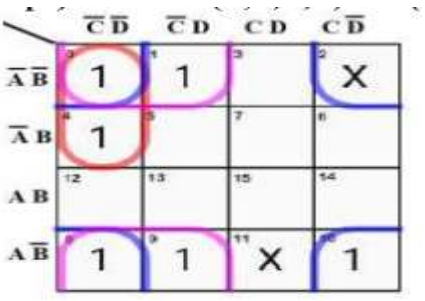
Q	Q^+ X = 0	Q^+ X = 1	T X = 0	T X = 1	Z
0	0	1	0	1	0
1	1	0	0	1	1

State Table for Parity Checker

Since only two states are required, a single flip-flop (Q) will suffice. We will let Q = 0 correspond to state S0 and Q = 1 corresponds to S1. We can then set up a table which shows the next state of flip-flop Q as a function of the present state and X. If we use a T flip-flop, T must be 1 whenever Q and Q^+ differ. From the above Table (b), the T input must be 1 whenever X = 1. The following Figure shows the resulting circuit.



$S = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{D} + \bar{B}\bar{C}$



$S = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{D} + \bar{B}\bar{C}$

	b. Find the minimum SOP for the function f (a, b, c, d) =∑m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14) using Quine-McCluskey method. Determine prime implicants **Solution:**	10	CO3	L3
6	a. With a block diagram explain the working of 4-bit parallel adder with accumulator **Solution:**	10	CO4	L2

Stage 1

Minterms	a b c d	
0	0000	✓
1	0001	✓
2	0010	✓
8	1000	✓
5	0101	✓
6	0110	✓
9	1001	✓
10	1010	✓
7	0111	✓
14	1110	✓

Stage 2

Minterms	a b c d	
0, 1	000–	✓
0, 2	00–0	✓
0, 8	–000	✓
1, 5	0–01	
1, 9	–001	✓
2, 6	0–10	✓
2, 10	–010	✓
8, 9	100–	✓
8, 10	10–0	✓
5, 7	01–1	
6, 7	011–	
6, 14	–110	✓
10, 14	1–10	✓

Stage 3

Minterms	a bcd
0, 1, 8, 9	–00–
0, 2, 8, 10	–0–0
~~0, 8, 1, 9~~	~~–00–~~
~~0, 8, 2, 10~~	~~–0–0~~
2, 6, 10, 14	– –1 0
~~2, 10, 6, 14~~	~~– –1 0~~

Prime implicant chart:

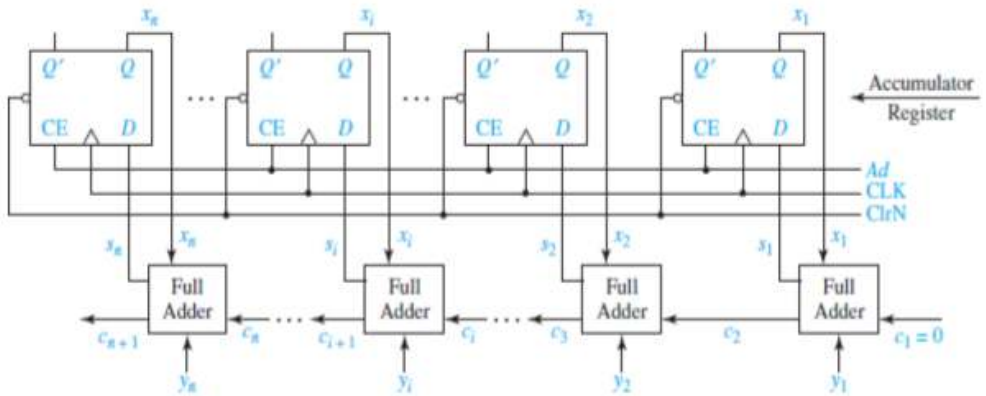
Prime Implecants		0	1	2	5	6	7	8	9	10	14
(0, 1, 8, 9)	b′c′	X	X					X	X		
(0, 2, 8, 10)	b′d′	X		X				X		X	
(2, 6, 10, 14)	cd′			X		X				X	X
(1, 5)	a′c′d		X		X						
(5, 7)	a′bd				X		X				
(6, 7)	a′bc					X	X				

$f = b'c' + cd' + a'bd$

Parallel Adder with Accumulator:

In computer circuits, it is frequently desirable to store one number in a register of flip-flops (called an accumulator) and add a second number to it, leaving the result stored in the accumulator.

One way to build a parallel adder with an accumulator is to add a register to the adder as shown in the following Figure.



Suppose that the number $X = x_n \ldots x_2x_1$ is stored in the accumulator. Then, the number $Y = y_n \ldots y_2y_1$ is applied to the full adder inputs, and after the carry has propagated through the adders, the sum of X and Y

appears at the adder outputs. An add signal (Ad) is used to load the adder outputs into the accumulator flip-flops on the rising clock edge. If $s_i = 1$, the next state of flip-flop x_i will be 1. If $s_i = 0$, the next state of flip-flop x_i will be 0.Thus, $x_i^+ = s_i$, and if $Ad = 1$, the number X in the accumulator is replaced with the sum of X and Y, following the rising edge of the clock.

Observe that the adder with accumulator is an iterative structure that consists of a number of identical cells. Each cell contains a full adder and an associated accumulator flip-flop. Cell i, which has inputs c_i and y_i and outputs $c_i = 1$ and x_i, is referred to as a typical cell.

Before addition can take place, the accumulator must be loaded with X. This can be accomplished in several ways. The easiest way is to first clear the accumulator using the asynchronous clear inputs on the flip-flops, and then put the X data on the Y inputs to the adder and add to the accumulator in the normal way. Alternatively, we could add multiplexers at the accumulator inputs so that we could select either the Y input data or the adder output to load into the accumulator. This would eliminate the extra step of clearing the accumulator but would add to the hardware complexity.

b. Design mod 5 counter using JK flip flops. | 10 | CO4 | L3

Solution:

Step 1:

Determine the number of flip flop needed

Flip flop required are

$2^n \geq N$

Mod 5 hence N=5

$\therefore 2^n \geq N$

$\therefore 2^n \geq 5$

$N = 3$ i.e. 3 flip flop are required

Step 2:

Type of flip flop to be used: JK flip flop

Step 3:

1) Excitation table for JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1

Now, we can derive excitation table for counter using above table as follows:

2) Excitation table for counter

Present state			Next state			Flip flop Input					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_a
0	0	0	0	0	1	×	0	0	×	1	×
0	0	1	0	1	0	×	1	1	×	×	1
0	1	0	0	1	1	×	×	×	0	1	×
0	1	1	1	0	0	×	×	×	1	×	1
1	0	0	0	0	0	1	0	0	×	0	×
1	0	1	×	×	×	×	×	×	×	×	×
1	1	0	×	×	×	×	×	×	×	×	×
1	1	1	×	×	×	×	×	×	×	×	×

Step 4

K-map simplification

For J_C

Q_BQ_A / Q_C	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_c = Q_BQ_A$

For K_C

Q_BQ_A / Q_C	00	01	11	10
0	X	X	X	X
1	1	X	X	X

$K_C = 1$

For K_B

Q_BQ_A / Q_C	00	01	11	10
0	×	×	1	0
1	×	×	×	×

$K_B = QA$

For J_A

Q_BQ_A / Q_C	00	01	11	10
0	1	×	×	1
1	0	×	×	×

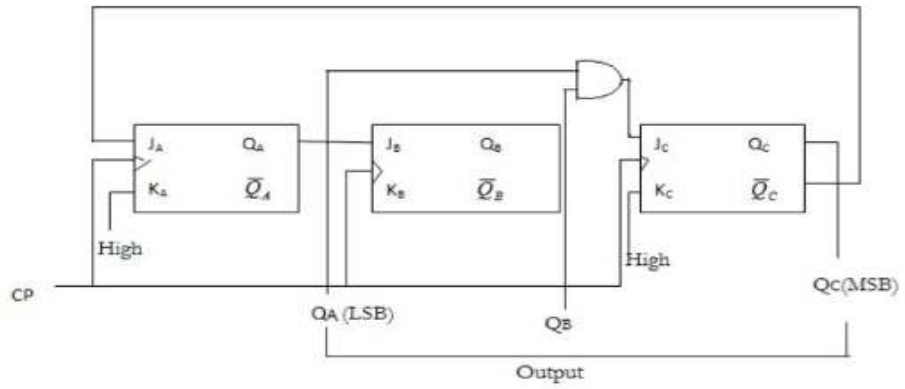
$J_A = \overline{Q}_C$

For K_A

Q_BQ_A / Q_C	00	01	11	10
0	×	1	1	×
1	×	×	×	×

$K_A = 1$

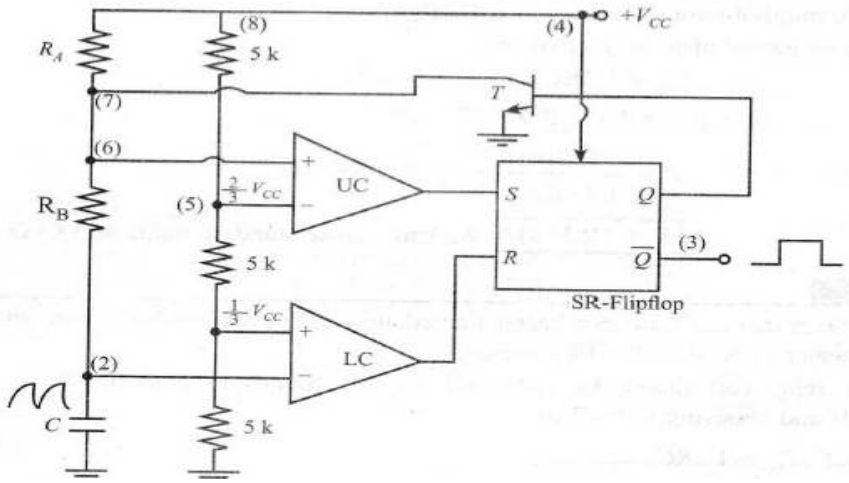
Step 5 Logic Diagram

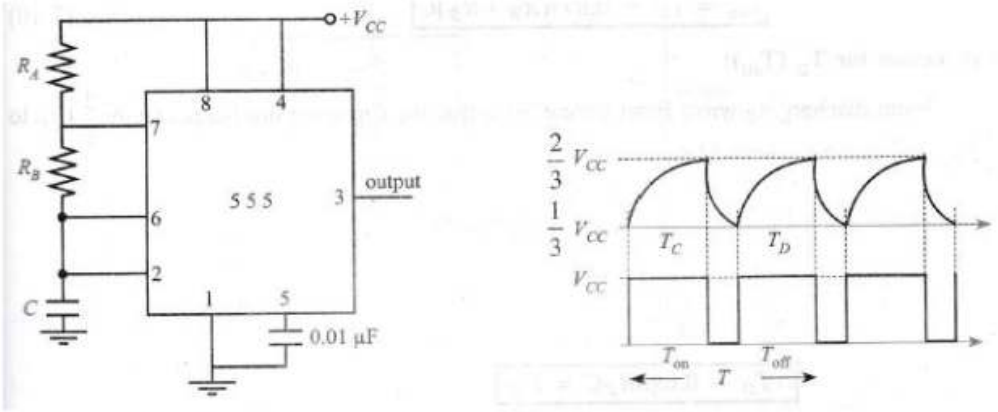


7	a. With a neat diagram and waveform, explain the working principle of astable multi vibrator using IC 555 timer.	10	CO1	L2

Solution:

An *astable multivibrator* does not have any stable state; it keeps changing its state from low to high and high to low. This multivibrator is also called *free running multivibrator* or *rectangular wave generator* circuit. *Astable multivibrator* does not require an external trigger pulse to change the state of the output. The circuit configuration of an astable multivibrator is as shown in the following Figure.





To understand the operation, let us divide the circuit operation into two time interval T_{ON} and T_{OFF}.

ON time operation:

- At $t = 0$, the voltage on the capacitor $V_{CC} = 0$, the same capacitor voltage is applied to both trigger point of lower comparator and threshold point of upper comparator. As capacitor voltage $V_C = 0$, which is less $1/3\ V_{CC}$, the output of lower comparator goes high ($\bar{Q} = 1$) and $Q = 0$. This

OFF time operation:

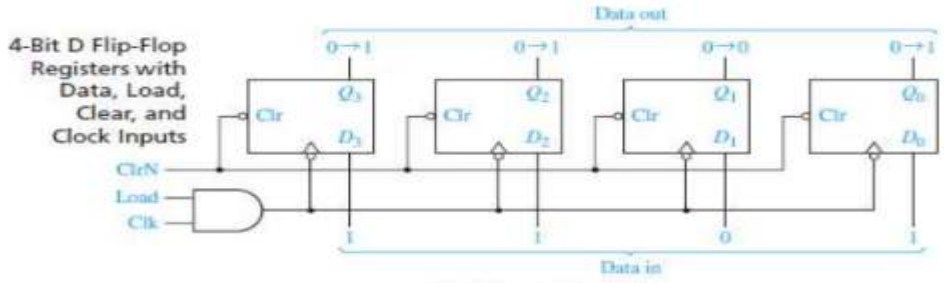
- As soon as V_C exceeds $2/3\ V_{CC}$, the upper comparator output goes high and it will set the SR FF. i.e., $S = 1$ and $R = 0$ and $Q = 1$ and $\bar{Q} = 0$. This will turn on transistor T, and output at pin (3) goes low.
- Now, the capacitor discharges through R_B, and through transistor T. The discharge time (also called off time (T_D); and it depends on the values of R_B and C. When capacitor voltage is $V_C = 1/3\ V_{CC}$, lower comparator output goes high.
- This process of charging and discharging is continuous and hence circuit oscillates. The schematic diagram and waveforms are as shown in the Above Figure.

b. Explain how 4 bits register with data, load, clear and clock input is constructed using D flip flops

10 | CO4 | L2

Solution:

Several D flip-flops may be grouped together with a common clock to form a register (SEE THE FOLLOWING Figure). Since each flip-flop can store one bit of information, this register can store four bits of information. This register has a load signal that is ANDed with the clock.



(a) Using gated clock

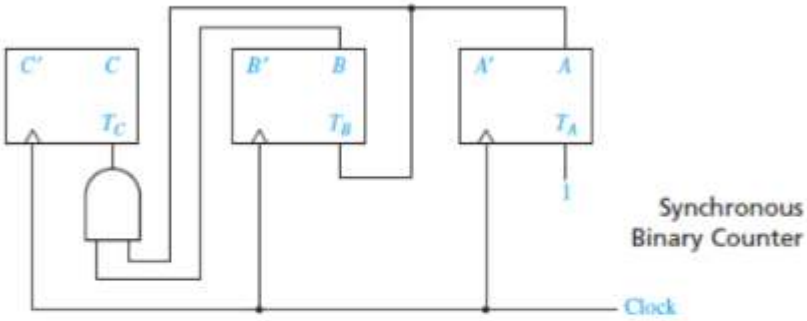
When Load = 0, the register is not clocked, and it holds its present value. Load = 1, the clock signal (Clk) is transmitted to the flip-flop clock inputs and the data applied to the D inputs will be loaded into the flip-flops on the falling edge of the clock.

For example, if the Q outputs are 0000 (Q3 = Q2 = Q1 = Q0 = 0) and the data inputs are 1101 (D3 = 1, D2 = 1, D1 = 0 and D0 = 1), after the falling edge of clock, Q will change from 0000 to 1101 as indicated in the above Figure (The notation 0 → 1 at the flip-flop outputs indicates a change from 0 to 1).

The flip-flops in the register have asynchronous clear inputs that are connected to a common clear signal, *ClrN*. The bubble at the clear inputs indicates that a logic 0 is required to clear the flip-flops. *ClrN* is normally 1, and if it is changed momentarily to 0, the Q outputs of all four flip-flops will become 0.

8	a. Design 3-bit synchronous binary counter using transition table of T flip flop. **Solution:**	10	CO4	L3

Synchronous Binary Counters Using T Flip-Flops: Consider the following Figure, a binary counter using three T flip-flops to count clock pulses.



Synchronous Binary Counter

All the flip-flops change state a short time following the rising edge of the input pulse. The state of the counter is determined by the states of the individual flip-flops; for example, if flip-flop C is in state 0, B in state 1, and A in state 1, the state of the counter is 011.

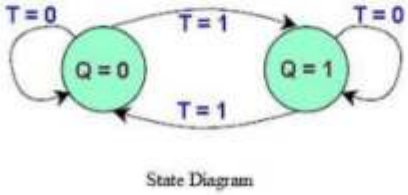
Initially, assume that all flip-flops are set to the 0 state. When a clock pulse is received, the counter will change to state 001; when a second pulse is received, the state will change to 010, etc. The sequence of flip-flop states is CBA = 000, 001, 010, 011, 100, 101, 110, 111, 000, . . . Note that, when the counter reaches state 111, the next pulse resets it to the 000 state, and then the sequence repeats.

State Table for Binary Counter

Present State			Next State			Flip-Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Table



State Diagram

$Q \rightarrow Q_{n+1}$		T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

	b. Using a 741 op-amp with a supply of 12V, design inverting Schmitt trigger circuit to have trigger points of ±2V **Solutions:**	10	CO1	L3

Given: $V_{cc} = \pm 12$ V, LTP = –2 V $C_2 \geq C_{B(max)}$, |LTP| = ±2 V

Let $C_2 = 50\ \mu A$, $V_{R_2} = UTP = +2$ V

$$R_2 = \frac{V_{R2}}{I_2} = \frac{2}{50 \times 10^{-6}} = 40\ k\Omega$$

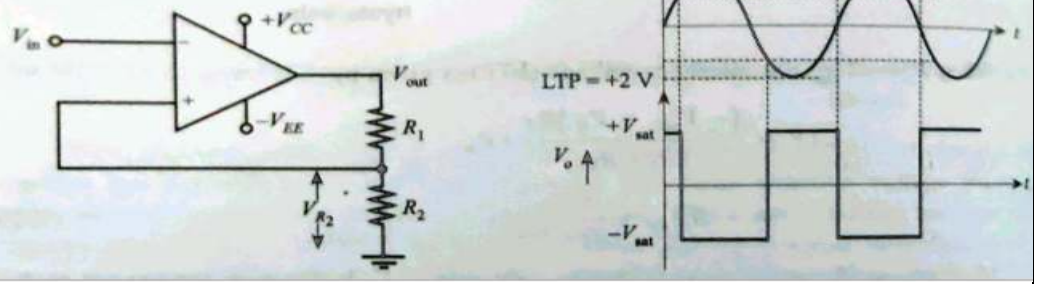
$$R_2 = 40\ k\Omega$$

$$R_1 = \frac{V_{0(sat)} - (\text{Trigger voltage})}{C_2}$$

$$R_1 = \frac{(12-1)-2}{50\times10^{-6}} = 180\ \text{k}\Omega \qquad \because V_{sat} = V_{CC} - 1$$

$$R_1 = 180\ \text{k}\Omega$$

Note: Above circuit used only if (UTP) = –|LTP|



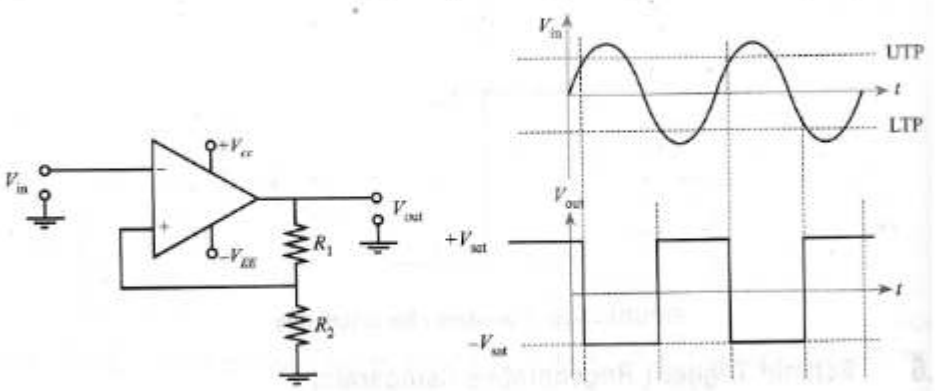
9	a. With hysteresis characteristics explain the working of Inverting Schmitt Trigger circuit.	10	CO1	L2

Solutions:

Inverting Schmitt Trigger:

The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback (i.e., feedback voltage aids the input voltage).

If the input voltage at the inverting terminal is slightly positive than feedback voltage at the non-inverting terminal, the output voltage will be negative (negative saturation, $-V_{sat}$); and if the input voltage more negative than the reference feedback voltage, the output will be positive (positive saturation, $+V_{sat}$).



Hence, the voltage at the output switches from $+V_{sat}$ to $-V_{sat}$ or vice-versa; are called *Upper Trigger Point (UTP)* and *Lower Trigger Point (LTP)*. The difference between two trigger points is called *Hysteresis*.

The upper and lower trigger points can be written as;

$$UTP = \frac{R_2}{(R_1+R_2)}\, e\, V_{sat} \qquad LTP = \frac{R_2}{(R_1+R_2)}\,(-V_{sat})$$

$$V_{hys} = UTP - LTP = \frac{R_2}{(R_1+R_2)}\, e\, V_{sat} - \frac{R_2}{(R_1+R_2)}\, e\,(-V_{sat}) = 2\left(\frac{R2}{R_1+R_2}\right)V_{sat} = 2\beta V_{sat}$$

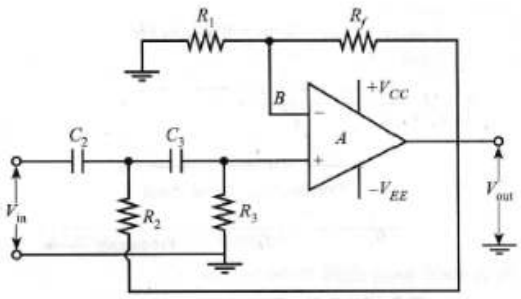
$$\beta = \frac{R2}{R_1+R_2}$$

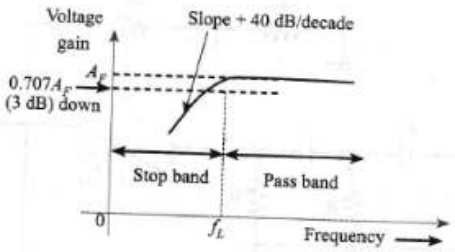
	b. Construct a 2nd order high pass filter with neat sketch and write its response curve	10	CO4	L2

Solutions:

Second Order High-Pass Filter:

A first order high-pass filter can be converted into a second order high-pass filter by using an extra RC-network in the input side. The frequency response of second order high-pass filter is same as the first order high-pass filter except that the gain at the stop band rolls off at the rate of 40 dB/decade.



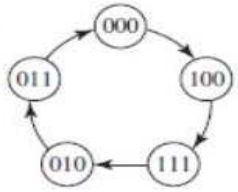


- The cut-off frequency is given by: $f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$.
  - If $R_2 = R_3 = R$ & $C_2 = C_3 = C$; then $f_L = \frac{1}{2\pi RC}$
- Pass band gain is given by: $A_F = 1 + \frac{R_f}{R_1}$

10 a. Design a random counter using T FF whose transition is 0 ⟶ 4 ⟶ 7 ⟶ 2 ⟶ 3 ⟶ 0 — 10 — CO4 — L23

Solutions:

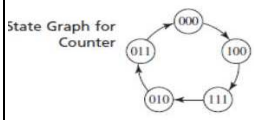
State Graph for Counter



State Table

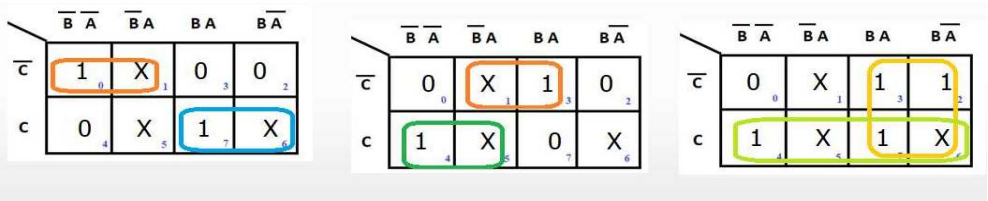
C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	–	–	–
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	0	1	0

Using T Flip Flop



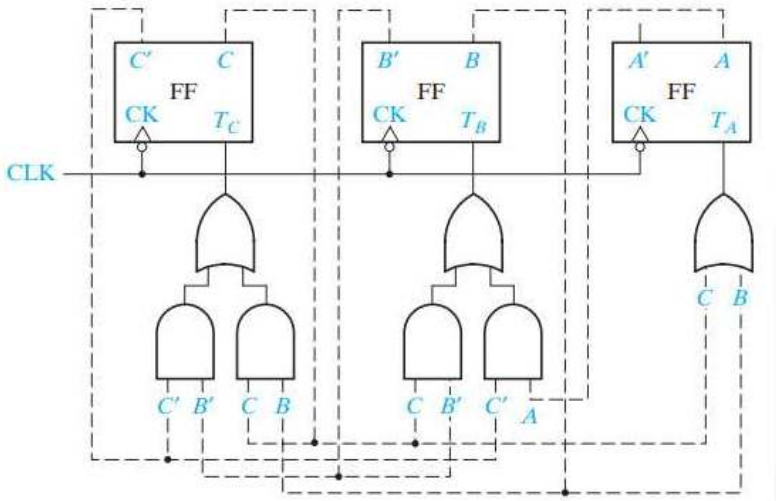
Present State			Next State			Flip-Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	1	0	0	1	0	0
0	0	1	-	-	-	x	x	x
0	1	0	0	1	1	0	0	1
0	1	1	0	0	0	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	-	-	-	x	x	x
1	1	0	-	-	-	x	x	x
1	1	1	0	1	0	1	0	1

Using T Flip Flop



$T_C = C'B' + CB$ $T_B = C'A + CB'$ $T_A = C + B$

$T_C = C'B' + CB$ $T_B = C'A + CB'$ $T_A = C + B$



b. With an example explain Petrik's method. | 10 | CO3 | L2

Solutions:

Steps in Petrick's method:

1. Reduce the prime implicant chart by eliminating the essential prime implicant rows and the corresponding columns.
2. Label the rows of the reduced prime implicant chart P_1, P_2, P_3, etc.
3. Form a logic function P which is true when all columns are covered. P consists of a product of sum terms, each sum term having the form $(P_{i0} + P_{i1} + \cdots)$, where P_{i0}, P_{i1} . . . represent the rows which cover column i.
4. Reduce P to a minimum sum of products by multiplying out and applying $X + XY = X$.
5. Each term in the result represents a solution, that is, a set of rows which covers all of the minterms in the table. To determine the minimum solutions, find those terms which contain a minimum number of variables. Each of these terms represents a solution with a minimum number of prime implicants.

6. For each of the terms found in step 5, count the number of literals in each prime implicant and find the total number of literals. Choose the term or terms which correspond to the minimum total number of literals, and write out the corresponding sums of prime implicants.

Determination of prime implicants:

Stage 1			Stage 2	
minterms	abc		*minterms*	abc
0	000	✓	0, 1	00–
1	001	✓	0, 2	0–0
2	010	✓	1, 5	–01
5	101	✓	2, 6	–10
6	110	✓	5, 7	1–1
7	111	✓	6, 7	11–

Prime implicant charts:

Prime Imlicants			0	1	2	5	6	7
P_1	(0, 1)	$a'b'$	X	X				
P_2	(0, 2)	$a'c'$	X		X			
P_3	(1, 5)	$b'c$		X		X		
P_4	(2 6)	bc'			X		X	
P_5	(5, 7)	ac				X		X
P_6	(6, 7)	ab					X	X

$P = (P_1 + P_2)(P_1 + P_3)(P_2 + P_4)(P_3 + P_5)(P_4 + P_6)(P_5 + P_6) = 1$

using $(X + Y)(X + Z) = X + YZ$ and distributive law:

$P = (P_1 + P_2P_3)(P_4 + P_2P_6)(P_5 + P_3P_6)$

$= (P_1P_4 + P_1P_2P_6 + P_2P_3P_4 + P_2P_3P_6)(P_5 + P_3P_6)$

$= P_1P_4P_5 + P_1P_2P_5P_6 + P_2P_3P_4P_5 + P_2P_3P_5P_6 + P_1P_3P_4P_6 + P_1P_2P_3P_6 + P_2P_3P_4P_6 + P_2P_3P_6$

use $X + XY = X$ to eliminate redundant terms from P.

$P = P_1P_4P_5 + P_1P_2P_5P_6 + P_2P_3P_4P_5 + P_1P_3P_4P_6 + P_2P_3P_6$

The two solutions with the minimum number of prime implicants are obtained by choosing rows P_1, P_4, and P_5 or rows P_2, P_3, and P_6.

F = a′b′ + bc′ + ac