CMR INSTITUTE OF TECHNOLOGY

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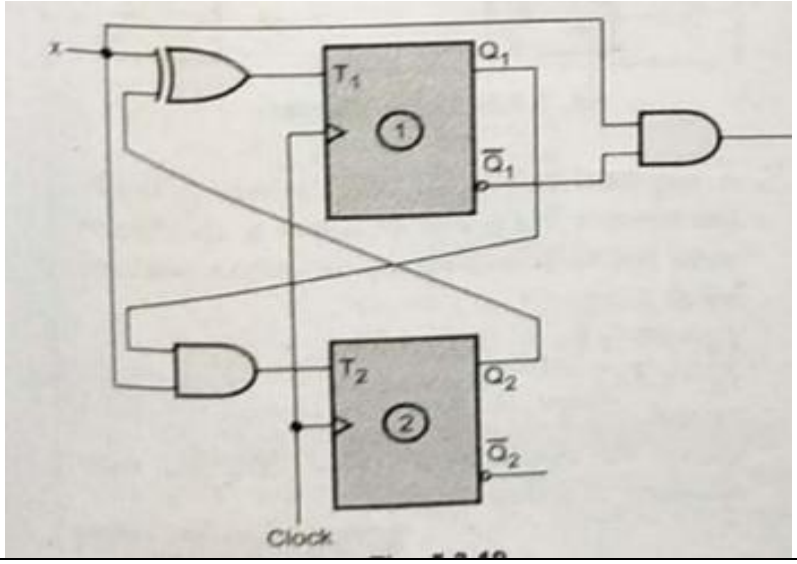
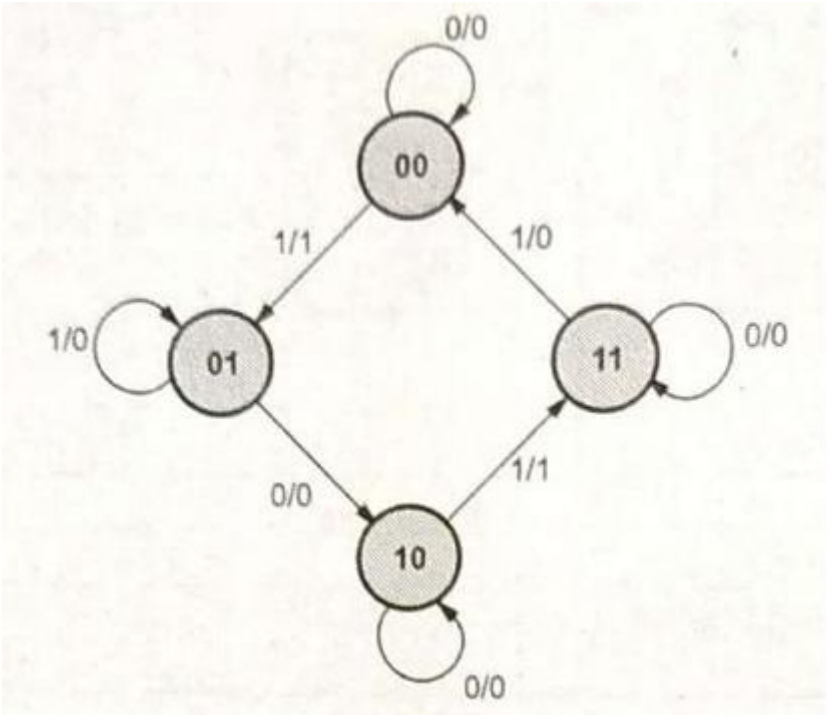
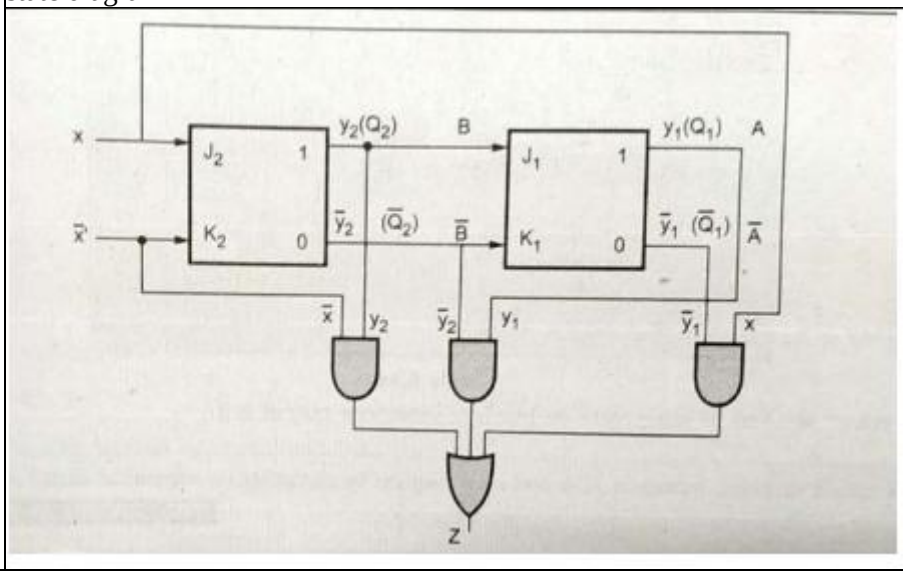
Internal Assesment Test - IV

Sub:	**DIGITAL SYSTEM DSESIGN**							Code:	18EE35
Date:	21/03/2022	Duration:	3 HRS	Max Marks:	100	Sem:	3rd	Branch:	EEE

Answer Any 10 Questions

		Marks	OBE	
			CO	RBT
1	Find a minimum SOP solution using Quine-McCluskey method F(a,b,c,d)=∑m(2,3,4,5,13,15) +d(8,9,10,11).	10	CO1	L3
2	Staircase light is controlled by two switches; one at the top of the stair and the other at the bottom of the stair: (a) Make a truth table for this system. (b) Write the logic equations in the POS form. (c) Realize the circuit using basic gates. (d) Realize the circuit using minimum number of NAND gates.	10	CO1	L2
3	Simplify the following using K-map and define combinational logic: Y=f(a,b,c,d)= πM (0,4,5,7,8,9,11,12,13,15).	10	CO1	L3
4	Simplify using K-Map Y=f(a,b,c,d,e)=∑m(1,3,4,6,9,11,12,14,17,1920,22,25,27,28,30)+ ∑d(8,10,2426)	10	CO1	L3
5	Differentiate synchronous and asynchronous counter. Mention the four different modes of operation shift registers.	10	CO3	L3
6	Design a Mod 6 ripple counter using T flip-flop.	10	CO3	L3
7	Design a synchronous counter with counting sequence 3,2,5,1,0,3...using D-flipflops	10	CO3	L3
8	With a neat logic diagram explain the different modes of operation of universal shift register	10	CO3	L3
9	Analyse the following sequential logic circuit shown in the figure below.Obtain the excitation and output equation,transition table and state table.Also draw a state diagram. 	10	CO4	L3

P.T.O

10	Construct a sequential circuit by obtaining the state and excitation table for the given diagrams using JK flipflop  	10	CO4	L3
11	Analyse the following sequential logic circuit shown in the figure below.Obtain the excitation and output equation,transition table and state table.Also draw a state diagram  	10	CO4	L3

CCI **HOD**

SOLUTION

1.

on : Step 1 : List all minterms in bina.; form.

Minterms	Binary representation			
m_2	0	0	1	0
m_3	0	0	1	1
m_4	0	1	0	0
m_5	0	1	0	1
m_{13}	1	1	0	1
m_{15}	1	1	1	1
dm_8	1	0	0	0
dm_9	1	0	0	1
dm_{10}	1	0	1	0
dm_{11}	1	0	1	1

Step 2 : Arrange the minterms according to number of 1's.

Minterms	Binary representation			
m_2	0	0	1	0
m_4	0	1	0	0
m_8	1	0	0	0
m_3	0	0	1	1
m_5	0	1	0	1
m_9	1	0	0	1
m_{10}	1	0	1	0
m_{11}	1	0	1	1
m_{13}	1	1	0	1
m_{15}	1	1	1	1

Step 3 :

Minterm			Binary representation			
2,	3	✓	0	0	1	–
2,	10	✓	–	0	1	0
4,	5		0	1	0	–
8,	10	✓	1	0	–	0
8,	9	✓	1	0	0	–
3,	11	✓	–	0	1	1
5,	13		–	1	0	1
9,	13	✓	1	–	0	1
9,	11	✓	1	0	–	1
10,	11	✓	1	0	1	–
13,	15	✓	1	1	–	1
11,	15	✓	1	–	1	1

Step 4 :

Minterm	Binary representation
2, 3, 10, 11	– 0 1 –
8, 9, 10, 11	1 0 – –
9, 11, 13, 15	1 – – 1

Step 5 :

Prime implicants	Binary representation
$\bar{a}$ b $\bar{c}$	4, 5	0 1 0 –
b $\bar{c}$ d	5, 13	– 1 0 1
$\bar{b}$ c	2, 3, 10, 11	– 0 1 –
a $\bar{b}$	8, 9, 10, 11	1 0 – –
a d	9, 11, 13, 15	1 – – 1

Step 6 :

Prime implicants		m_2	m_3	m_4	m_5	m_{13}	m_9	dm_8	dm_9	dm_{10}	dm_{11}
$\bar{a}$ b $\bar{c}$	4, 5			⊙	⊙						
b $\bar{c}$ d	5, 13				•	•					
$\bar{b}$ c	2, 3, 10, 13	⊙	⊙			⊙				⊙	
a $\bar{b}$	8, 9, 10, 11							•	•	•	•
a d	9, 11, 13, 15					⊙	⊙		⊙		⊙

∴ $Y = \bar{b}c + \bar{a}b\bar{c} + ad$

2.

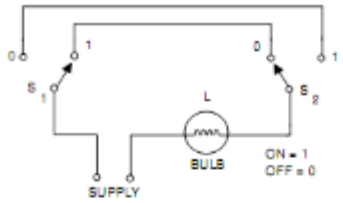


Fig.(a) Circuit diagram

a. The truth table for the system is illustrated in given truth table

S1	S2	L
0	0	0
0	1	1
1	0	1
1	1	0

b. The logic equation for given system is specified by $L = S_1\bar{S}_2 + S_1\bar{S}_2$

c. Realization of given case, the circuit using AND-OR gates is demonstrated in fig (b)

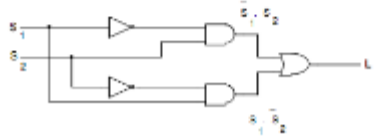
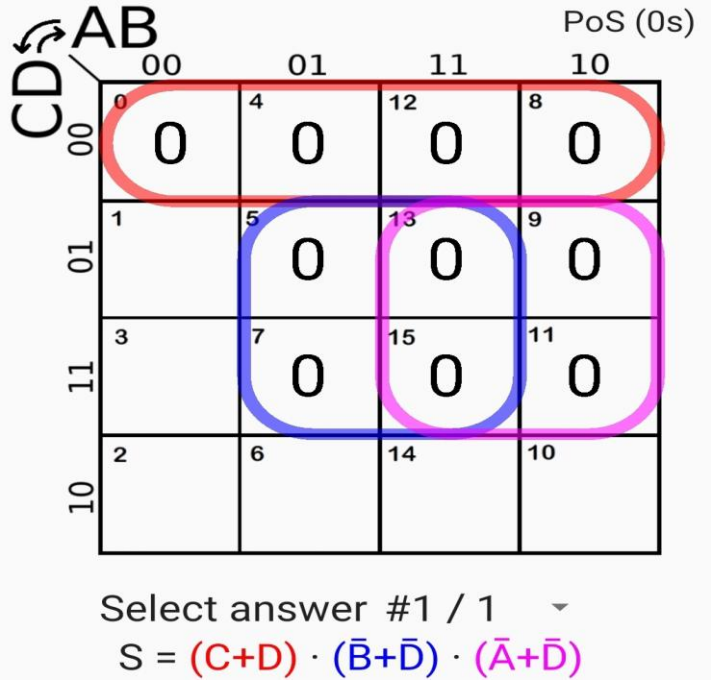
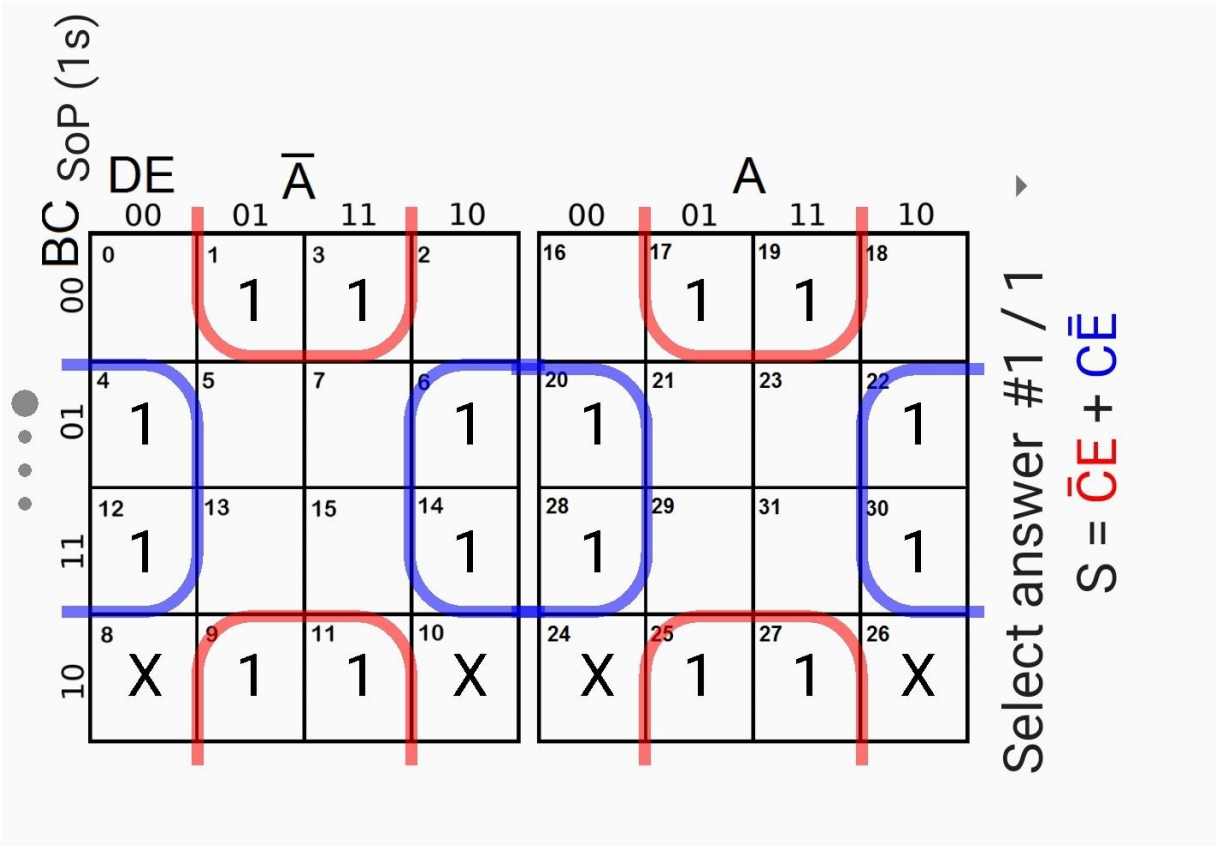


Fig.(b) Logic Diagram for the system

3.


PoS (0s)
AB
CD
00 01 11 10
0 4 12 8
0 0 0 0
1 5 13 9
0 0 0
3 7 15 11
0 0 0
2 6 14 10
Select answer #1 / 1
S = (C+D) · (B̄+D̄) · (Ā+D̄)

4.


SoP (1s)
BC
DE
Ā
A
00 01 11 10
0 1 3 2
1 1
4 5 7 6
1 1
12 13 15 14
1 1
8 9 11 10
X 1 1 X
16 17 19 18
1 1
20 21 23 22
1 1
28 29 31 30
1 1
24 25 27 26
X 1 1 X
Select answer #1 / 1
S = C̄E + CĒ

5.

Difference between Synchronous and Asynchronous Counter

S.No.	Synchronous Counter	Asynchronous Counter
1.	In the synchronous counter there are continuous clock input signals with flip-flops used to produce the output.	In Asynchronous counters there are different clock signals used to produce the output.
2.	In the synchronous counter, the operation is faster.	In Asynchronous counter the operation is slower.
3.	Synchronous counter is also known as Parallel counter.	Asynchronous counter is also known as Serial counter.
4.	Synchronous counter produces less error than asynchronous counter.	Asynchronous counter produces more errors than a synchronous counter.
5.	Design of the Synchronous counter is complex.	Design of the Asynchronous counter is simple.
6.	Synchronous counters can work with a flexible number of count sequences.	Asynchronous counters can work with a fixed number of count sequences.

There are four basic modes of operation based on the movement of data in the Registers and they are:

- Serial In – Serial Out (SISO) Mode.
- Serial In – Parallel Out (SIPO) Mode.
- Parallel In – Serial Out (PISO) Mode.
- Parallel In – Parallel Out (PIPO) Mode.

6.

Solution :

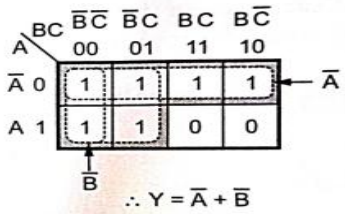
Step 1 : Determine the number of flip-flop required. Here, counter goes through 0 - 5 states, i.e., total 6 states. Thus N = 6 and for $2^n \geq N$ we need n = 3, i.e. 3 flip-flops.

Step 2 : Type of flip-flops to be used : T

Step 3 : Write the truth table for counter

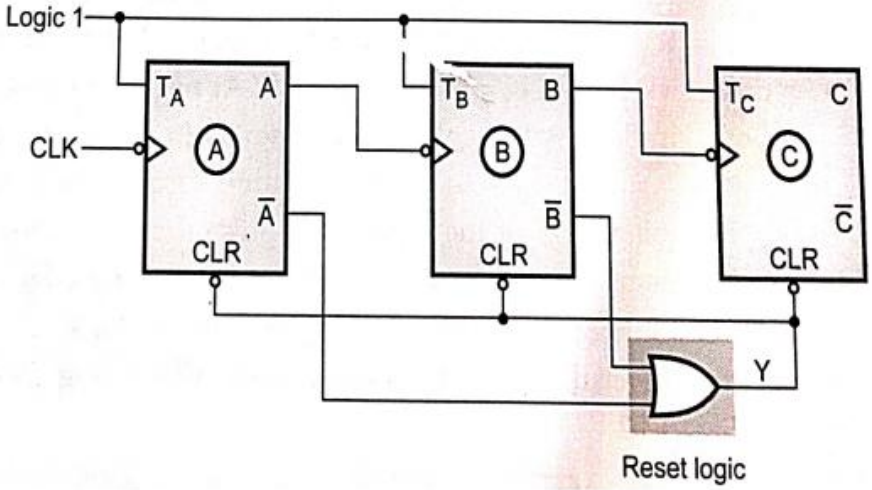
CLK	A	B	C	Output of reset logic Y	
0	0	0	0	1	Valid states
1	0	0	1	1	
2	0	1	0	1	
3	0	1	1	1	
4	1	0	0	1	
5	1	0	1	1	
–	1	1	0	0	Invalid states
–	1	1	1	0	

Step 4 : Derive reset logic



$\therefore Y = \overline{A} + \overline{B}$

Step 5 : Draw logic diagram

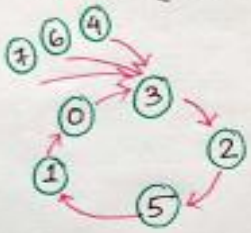


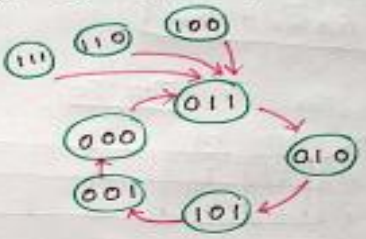
Reset logic

7.

⇒ Here maximum count is 5. 5 = $(101)_2$. Th consists of 3 Bits. So, number of flip flops be 3.

** We are considering that whenever counte an invalid state, then it will reset to value (i.e 3).

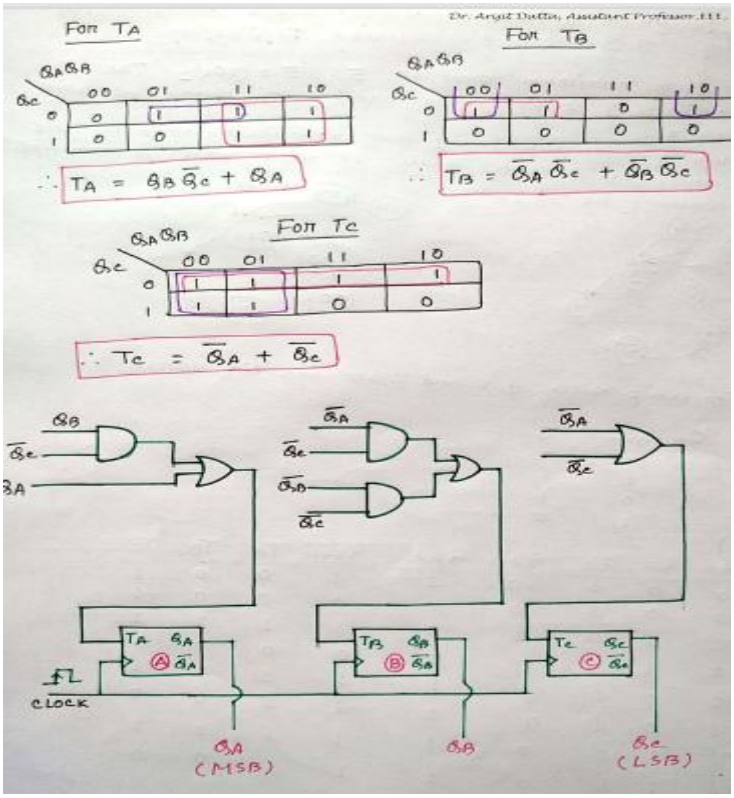




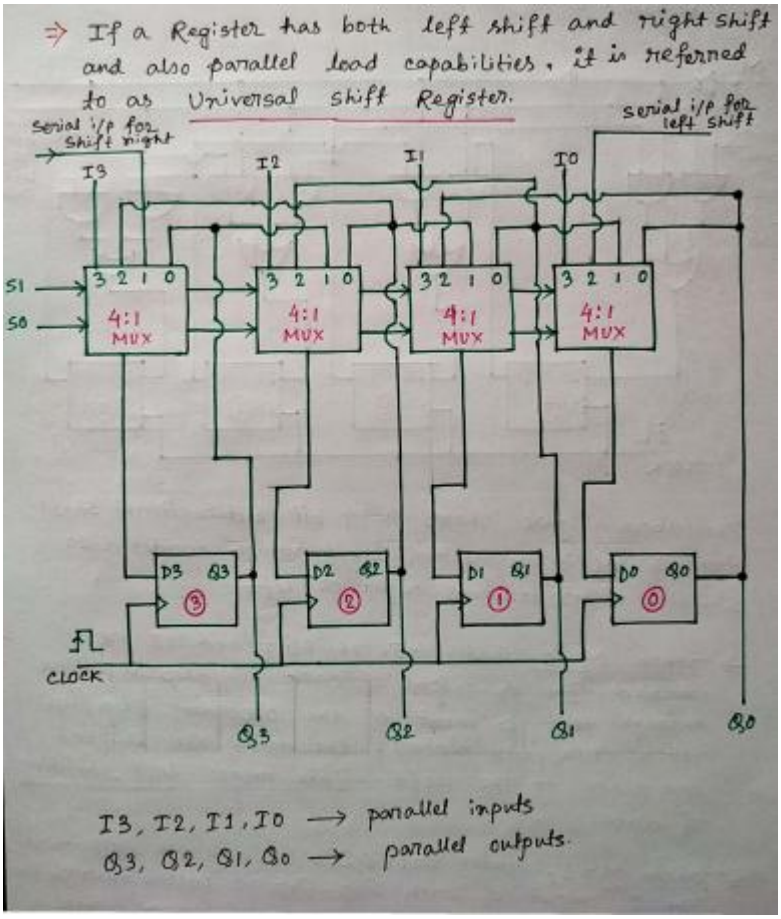
For this problem, 4, 6 and 7 are invalid states.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	0	1
0	1	0	1	0	1	1	1	1
0	1	1	0	1	0	0	0	1
invalid 1	0	0	0	1	1	1	1	1
1	0	1	0	0	1	1	1	0
invalid 1	1	0	0	1	1	1	1	0
valid 1	1	1	0	1	0	1	1	0


Dr. Arijit Dutta, Assistant Professor, EE
For TA
For TB
For Tc
TA = QB Q̄c + QA
TB = Q̄A Q̄c + Q̄B Q̄c
Tc = Q̄A + Q̄c
CLOCK
QA (MSB)
QB
Qc (LSB)

8.


If a Register has both left shift and right shift and also parallel load capabilities, it is referred to as Universal Shift Register.
serial i/p for shift right
serial i/p for left shift
I3
I2
I1
I0
S1
S0
4:1 MUX
CLOCK
Q3
Q2
Q1
Q0
I3, I2, I1, I0 → parallel inputs
Q3, Q2, Q1, Q0 → parallel outputs.

→ 9T consists of 4 flip flops and 4 Multiplexers. The four Multiplexers have two common select inputs S1 and S0. and they select appropriate input for D flip-flop. The below table shows the register operation depending on the select lines of multiplexer.

Mode control		Register Operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	parallel Load.

→ When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in Register value.

→ When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift Register.

→ When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift Register.

→ Finally when $S_1S_0 = 11$, the binary information on the parallel input lines is transfered into the register simultaneously and it is a parallel load operation.

9.

Sol. : Step 1 : Excitation and output equations.

$$Z = x\bar{Q}_1$$

$$T_1 = x\bar{Q}_2 + \bar{x}Q_2 = x \oplus Q_2$$

$$T_2 = xQ_1$$

Step 2 : Transition equations

The transition equation for T flip-flop is,

$$Q^+ = T \oplus Q$$

$$Q_1^+ = x \oplus Q_2 \oplus Q_1$$

$$Q_2^+ = xQ_1 \oplus Q_2$$

Step 3 : Next state map for each flip-flop

For Q_1^+

Q_2Q_1 \ x	0	1
00	0	1
01	1	0
10	1	0
11	0	1

For Q_2^+

Q_2Q_1 \ x	0	1
00	0	0
01	0	1
10	1	1
11	1	0

K-Ma not Requir

Step 4 : Excitation table

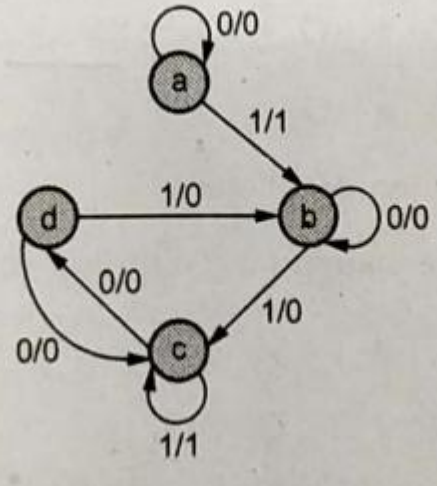
Present state		Next state				Output Z	
Q_2	Q_1	x = 0		x = 1		x = 0	x = 1
		Q_2^+	Q_1^+	Q_2^+	Q_1^+		
0	0	0	0	0	1	0	1
0	1	0	1	1	0	0	0
1	0	1	1	1	0	0	1
1	1	1	0	0	1	0	0

Step 5 : State table

Assuming a = 00, b = 01, c = 10 and d = 11 we have

Present state	Next state		Output Z	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	1
b	b	c	0	0
c	d	c	0	1
d	c	b	0	0

Step 6 : State diagram



10.

Fig. 5.5.37

∴ 2 F/F

Sol. :

Step 1 : State table

Present state		Next state		Output	
		x = 0	x = 1	x = 0	x = 1
A	B	A_+ B_+	A_+ B_+	Y	Y
0	0	0 0	0 1	0	1
0	1	1 0	0 1	0	0
1	0	1 0	1 1	0	1
1	1	1 1	0 0	0	0

Table 5.5.27

Step 2 : K-map simplification :

$$D_A = \bar{x}B + A\bar{B}$$

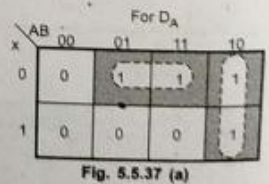


Fig. 5.5.37 (a)

$$D_B = \bar{x}AB + x\bar{A} + x\bar{B}$$

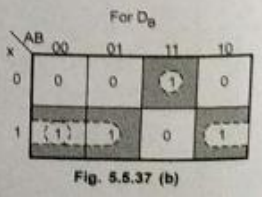


Fig. 5.5.37 (b)

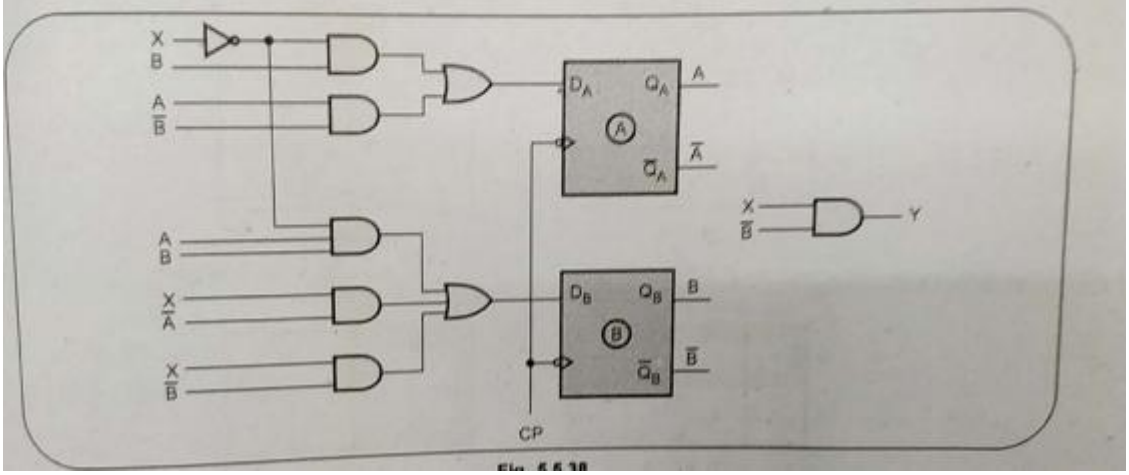
$$Y = x\,\overline{B}$$

For Y

x \ AB	00	01	11	10
0	0	0	0	0
1	1	0	0	1

Fig. 5.5.37 (:)

Sequential circuit :



11.

Fig. 5.3.13

Sol. : The flip-flop input equations and output equations are,

$J_2 = x \quad J_1 = y_2$ and $z = \overline{x}\,y_2 + \overline{y_2}\,y_1 + \overline{y_1}\,x$

$K_2 = \overline{x} \quad K_1 = \overline{y_2}$

For JK flip-flop, $Q^+ = J\overline{Q} + \overline{K}Q$

$J_2^+ = Q_2^+ = J_2\overline{Q}_2 + \overline{K}_2 Q_2$

$= x\overline{Q}_2 + xQ_2 = x\overline{y}_2 + xy_2$

$J_1^+ = Q_1^+ = J_1Q_1 + \overline{K}_1Q_1$

$= y_2\overline{Q}_1 + \overline{\overline{y_2}}Q_1$

$= y_2\overline{y}_1 + y_2 y_1$

$= y_2(\overline{y}_1 + y_1) = y_2$

Next-state maps of each flip-flop.

For J_2^+

y_2y_1 \ x	0	1
00	0	1
01	0	1
10	0	1
11	0	1

$J_2^+ = x$

For J_1^+

y_2y_1 \ x	0	1
00	0	0
01	0	0
10	1	1
11	1	1

$J_1^+ = y_2$

K-Map is not require

Fig. 5.3.13 (a)

Present state		Next state				Output z	
		x = 0		x = 1		x = 0	x = 1
y_2	y_1	y_2^+	y_1^+	y_2^+	y_1^+		
0	0	0	0	1	0	0	1
0	1	0	0	1	0	1	1
1	0	0	1	1	1	1	1
1	1	0	1	1	1	1	0