CBCS SCHEME

USN

18EE35

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the definition of combinational logic. Convert the given Boolean expression into minterm canonical form and maxterm canonical form.

$F(x,y,z) = X + \bar{x}\,\bar{z}(y+z)$. **(08 Marks)**

b. Simplify the function :
$Y = f(a, b, c, d) = \Sigma m(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$ using Karnaugh map. **(06 Marks)**

c. Simplify the function :
$Y = f(a, b, c, d) = \pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ using the Karnaugh map. **(06 Marks)**

OR

2 a. Simplify wing the Quine – McClusky minimization technique :
$Y = f(a, b, c, d) = \Sigma m(0, 2, 8, 10)$. **(08 Marks)**

b. Using the Quine – McCluskey method, obtain all the prime implicates for the following Boolean function :
$f(a, b, c, d) = \pi M(0, 2, 3, 4, 5, 12, 13) + dc(8, 10)$. **(12 Marks)**

Module-2

3 a. With the aid of general structure, clearly distinguish between a decoder and encoder. **(06 Marks)**

b. Implement the following Boolean function using 4 : 1 multiplexer.
$F(A, B, C) = \Sigma m(1, 3, 5, 6)$ **(06 Marks)**

c. Implement full subtractor using a decoder and two NAND gates and write its truth table. **(08 Marks)**

OR

4 a. What is carry look ahead adder? Explain general organization of it. **(06 Marks)**

b. Write a truth table for two – bit magnitude comparator. Write the Karnaugh map for each output of two bit magnitude comparator and the resulting equation. **(14 Marks)**

Module-3

5 a. What is a Flip-Flop? Discuss the working principle of SR Flip Flop with its truth table. Also high light the role of SR Flip Flop in switch debouncer circuit. **(12 Marks)**

b. Explain the operation of Master - Slave JK flip-flop along with its circuit diagram. **(08 Marks)**

OR

6 a. Draw and explain the working of Positive and Negative edge triggered D flip-flop. **(12 Marks)**

b. Derive the characteristic equations for D, JK, T and SR flip flops. **(08 Marks)**

Module-4

7 a. Explain with suitable logic and timing diagram :
i) Serial–in serial–out shift register
ii)Parallel–in parallel out shift register. **(10 Marks)**

b. Compare Registers and Counters. Explain the working of 4-bit Asynchronous counter using JK flip-flops. **(10 Marks)**

OR

8 a. Describe the block diagram of a MOD – 7 Jonson counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. **(10 Marks)**

b. Design a MOD – 5 synchronous binary counter using clocked J-K flip-flops. **(10 Marks)**

Module-5

9 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. **(08 Marks)**

b. A sequential circuit has one input and one output. The state diagram is as shown in Fig.Q9(b). Design a sequential circuit with 'T' flip-flop.

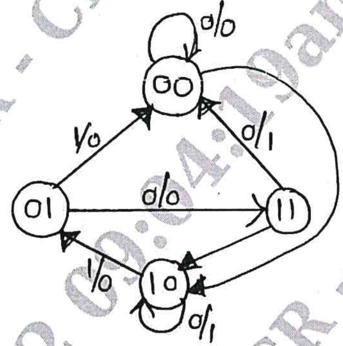


Fig.Q9(b) **(12 Marks)**

OR

10 a. With a basic structure, explain clearly Programmable Read Only Memories (PROMS) and EPROM. **(13 Marks)**

b. Write short note on :
i) Read only and Read/Write memories
ii) Flash memory. **(07 Marks)**

* * * * *

Module 1

1a. Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are following −

- The output of combinational circuit at any instant of time, depends only on the levels present at input terminals.
- The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

Block diagram

$F(x,y,z) = x + \bar{x}\bar{z}(y+z)$	$= x + \bar{x}\bar{z}y + \cancel{\bar{x}\bar{z}z}$
$= (x+\bar{x}\bar{z})[x+(y+z)]$	$= x + \bar{x}y\bar{z}$
$= (x+\bar{z}+y)(x+\bar{z}+\bar{y})(x+y+z)$	$= x(y+\bar{y})(z+\bar{z}) + \bar{x}y\bar{z}$
$f = M_0 . M_1 . M_2$	$f = m_2 + m_4 + m_5 + m_6 + m_7$

b.

$$(a)\quad F_1(a,b,c,d) = \Sigma m(2,3,4,5,13,15) + \Sigma d(8,9,10,11)$$

$$F_1 = A'BC' + B'C + AD$$

AB \ CD				
			1	1
	1	1		
		1	1	
	X	X	X	X

c.

(c)	$y = (c+d)(c'+d')(b'+d')$

2.

2(a)

Group	term	a	b	c	d
0	0	0	0	0	0 ✓
1	2	0	0	1	0 ✓
1	8	1	0	0	0 ✓
2	10	1	0	1	0 ✓

Group	term	a	b	c	d
0	0,2	0	0	-	0
0	0,8	-	0	0	0
1	2,10	-	0	1	0
1	8,10	1	0	-	0
0	0,2,8,10	-	0	-	0 PI

$\boxed{y = b'd'}$ ← (1)

(2) (3) (2)

2+3
2+1
= 08

(b) For prime implicates don't care cells as '0' cells } — 01

$\therefore f(a,b,c,d) = \Pi M(0,2,3,4,5,8,10,12,13)$

$\therefore \bar{f}(a,b,c,d) = \overline{M_0 \cdot M_2 \cdot M_3 \cdot M_4 \cdot M_5 \cdot M_8 \cdot M_{10} \cdot M_{12} \cdot M_{13}}$

$= \bar{M}_0 + \bar{M}_2 + \bar{M}_3 + \bar{M}_4 + \bar{M}_5 + \bar{M}_8 + \bar{M}_{10} + \bar{M}_{12} + \bar{M}_{13}$ } — 02

$= m_0 + m_2 + m_3 + m_4 + m_5 + m_8 + m_{10} + m_{12} + m_{13}$

$\therefore \bar{f}(a,b,c,d) = \Sigma m(0,2,3,4,5,8,10,12,13)$

Const. of QMC table in 1/0 notation .... → 03

No	Minterm	1/0 notation	Index
0	$\bar{a}\bar{b}\bar{c}\bar{d}$	0 0 0 0	0
2	$\bar{a}\bar{b}c\bar{d}$	0 0 1 0	2
⋮	⋮	⋮	⋮
13	$ab\bar{c}d$	1 1 0 1	3

Const. of steps (2&3) → 02

All further steps → 02

prime imp. of $\bar{f}$ without		prime implicates of f	
$\bar{a}\bar{b}c$	$c\bar{d}$	$a+b+\bar{c}$	$\bar{c}+d$
$\bar{b}\bar{d}$	$b\bar{c}$	$b+d$	$\bar{b}+c$

— 02

= 12

Module 2

3a.

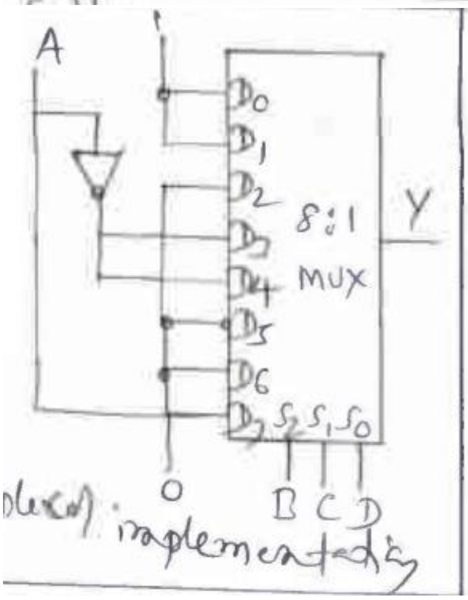
S.NO.	ENCODER	DECODER
1.	The combinational circuits that modify the binary data into N output lines are known as Encoders.	The combinational circuits that convert the binary data into 2N output lines are called Decoders.
2.	In this the output lines are n.	In this the output lines are 2n.
3.	The implemented signal is considered as actual signal input.	It receives coded binary data as its input.
4.	It is utilized in videos, E-mail, and more.	It is mostly utilized in memory chips, microprocessors, and more.
5.	When it comes to the communication mode, the encoder is situated at the transmitting end.	Here, the decoder is situated at the receiving side.
6.	The operating procedure is quite simple here.	The operating procedure is complex.

b.

(b)

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A

Implementation table



plexer implementation

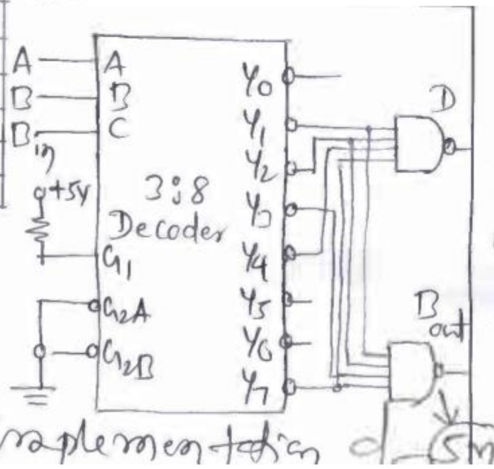
02 + 04 = 06

c.

(c)

Inputs			outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Truth table - 03

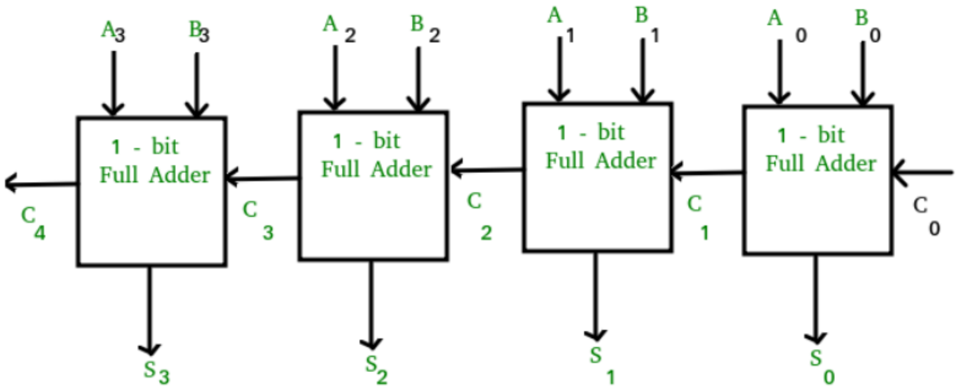


03 + 05 = 08

Implementation d - (5M)

4a.

In ripple carry adders, for each adder block, the two bits that are to be added are available instantly. However, each adder block waits for the carry to arrive from its previous block. So, it is not possible to generate the sum and carry of any block until the input carry is known. The i^{th}block waits for the $i-1^{th}$block to produce its carry. So there will be a considerable time delay which is carry propagation delay.



Consider the full adder circuit shown above with corresponding truth table. We define two variables as **'carry generate'** $G_i$and **'carry propagate'** $P_i$then,

$$P_i = A_i \oplus B_i$$
$$G_i = A_i B_i$$

The sum output and carry output can be expressed in terms of carry generate $G_i$and carry propagate $P_i$as

$$S_i = P_i \oplus C_i$$
$$C_{i+1} = G_i + P_i C_i$$

where $G_i$produces the carry when both A_i, $B_i$are 1 regardless of the input carry. $P_i$is associated with the propagation of carry from $C_i$to C_{i+1}.

The carry output Boolean function of each stage in a 4 stage carry look-ahead adder can be expressed as

$$C_1 = G_0 + P_0 C_{in}$$
$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{in}$$
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$$
$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{in}$$

4(b) 1. solution for outputs $(A=B) = \Sigma(0,5,10,15)$

$(A>B) = \Sigma(4,8,9,12,13,14)$ — 04

$(A<B) = \Sigma(1,2,3,6,9,11)$

2 K-maps ---------------- 06

3 Resulting Equation

$(A=B) = a_1'a_0'b_1'b_0' + a_1'a_0b_1'b_0 + a_1a_0b_1b_0 + a_1a_0'b_1b_0'$

$(A>B) = a_1b_1' + a_0b_1'b_0' + a_1a_0b_0'$ — 04

$(A<B) = a_1'b_1 + a_1'a_0'b_0 + a_0'b_1b_0$

14

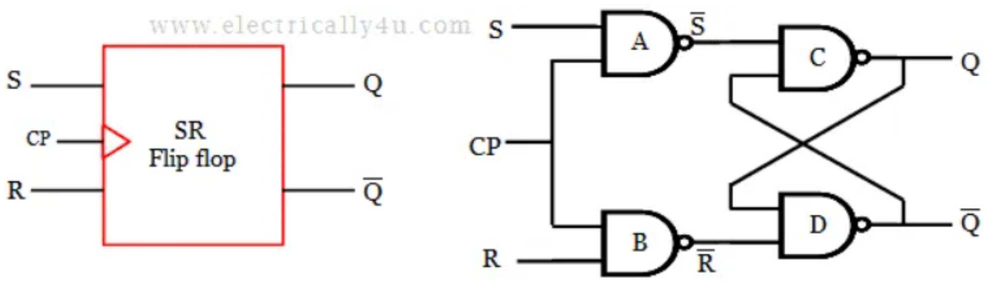
Module 3

5a. A flip-flop is **a device which stores a single bit (binary digit) of data**; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics. SR flip flop, also known as SR latch is the basic and simplest type of flip flop. It is a single bit storage element. It has only two logic gates. The output of each gate is connected to the input of another gate.

The state of the SR flip flop is determined by the condition of the output Q. If its value is 1, then the state is said to be SET and if Q = 0, the state is said to be RESET. Hence it is called SR flip flop.

The Clocked SR flip-flop consists of 4 NAND gates, two inputs(S and R) and two outputs(Q and Q'). The clock pulse is given at the inputs of gate A and B.

If the clock pulse input is replaced by an enable input, then it is said to be SR latch. Let us assume that this flip flop works under positive edge triggering. The following figure shows the block diagram and the logic circuit of a clocked SR flip flop.



Clocked SR flip flop

For interfacing keys to the digital systems, push bottom keys are used. Such push button key when pressed bounces a few seconds and then after few times it comes back to its initial position automatically during stable state. But before coming in to stable state if we take output then such output may be faulty. This problem is known as key debounce. It is undesirable and must be avoided.

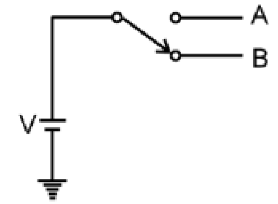
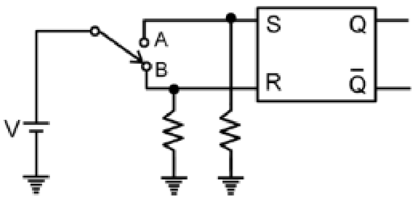
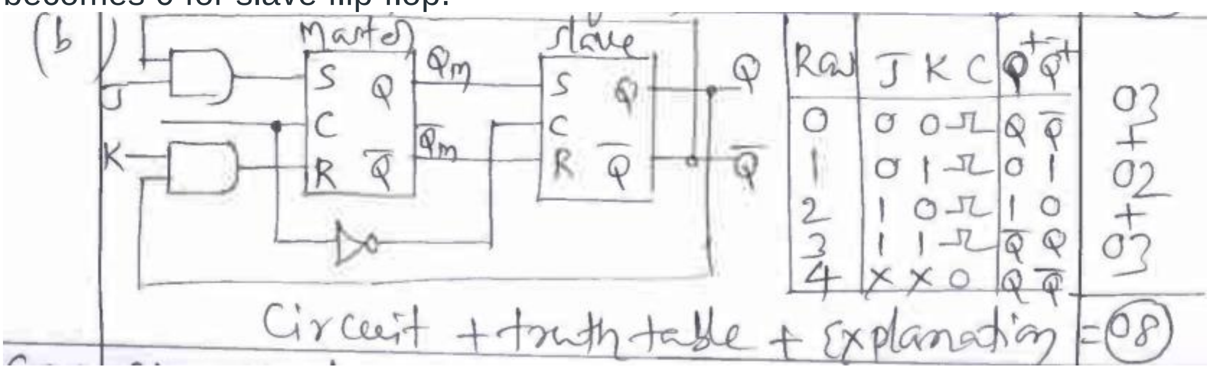


Fig 7.3 Key bouncing switch.

One way to avoid key debounce problem is to use S-R latch. The circuit where S-R latch is used to avoid key bounce is called a switch debouncer.



b. The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **"master"** and the other as a **"slave"**. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.
In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.



6(a) Circuit diagram + Working of positive & Negetive edge triggered D-flip-flop — 06 + 06 = (12)

(b) characteristic equations

D, $Q_{n+1} = D$ ..., $\overline{J}K$, $Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$ — 02+02

T, $Q_{n+1} = T\overline{Q}_n + \overline{T}Q_n$, SR, $Q_{n+1} = S + \overline{R}Q_n$ — 02+02 =(08)

Module 4

7(a) Serial in serial out shift register

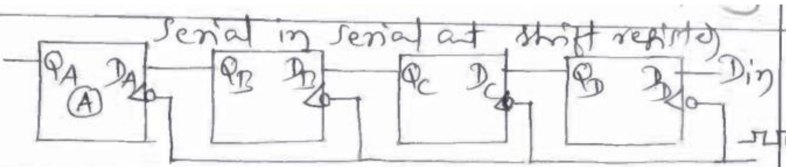
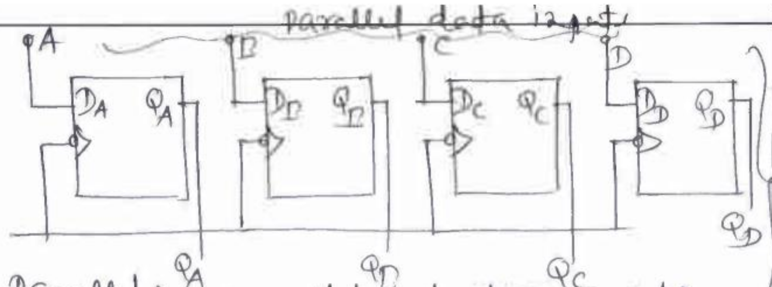


DIAGRAM + EXPLANATION — 05

Parallel data input



Parallel in parallel out shift register

DIAGRAM + EXPLANATION -05- =(10)

7(b) → A group of FF's connected together forms a register. A register is used solely for storing and shifting data in 1's or 0's form — 01

Counter is a register capable of counting the no. of clock pulses arriving at its clock I/p. A specified sequence of states appears as the counter output. — + 01

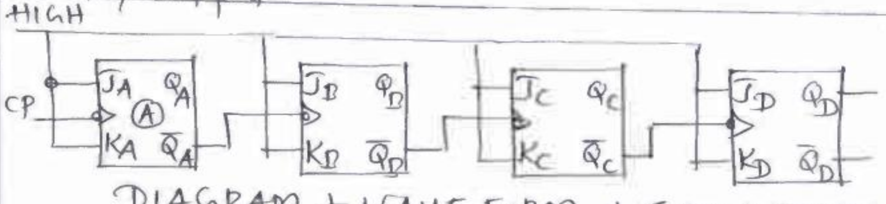


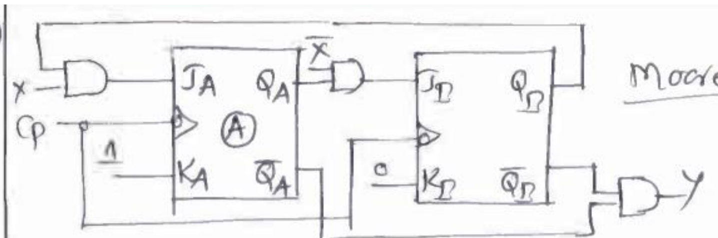
DIAGRAM + WAVEFORM + EXPLANATION
-03- + -03- + -02-

+ 03 + 03 + 02 =(10)

		−(10)
8 (a)	In Johnson counter, the Q output of each stage of flip-flop is connected to the D input of the next stage. DIAGRAM, truth table, Explanation & timing diagram.	2+2 3+3 =10
(b)	Flip-flop required $2^n \geq N$, $N=5$, $n=3$ (1) Excitation table for JK, (2) transition table (3) K-map (4) Logic-diagram (5) timing diagram	=2×5 =10

Module 5

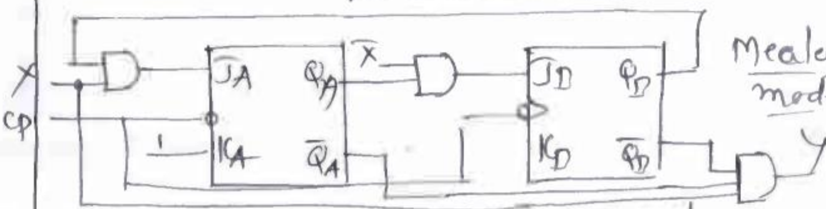
9(a)



Moore model

04

+



Mealey model

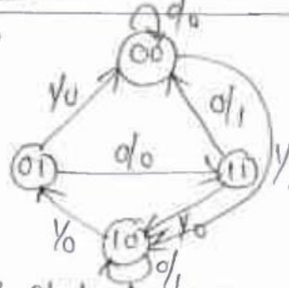
04

=(08)

9(b) Excitation of a T-flip-flop

$Q_n \rightarrow Q_{n+1}$	T
0 → 0	0
0 → 1	1
1 → 0	1
1 → 1	0

(1)



Give state diagram

Excitation
−01−

+

Present state Q_A	Q_B	Input X	Next state A	B	Flip-flop inputs T_A	T_B	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0

03 +

	$\bar{B}\bar{X}$	$\bar{B}X$	BX	$B\bar{X}$
$\bar{A}$	0	1	1	0
A	1	0	0	1

0	0	1	0
0	1	1	1

output Y

0	0	1	1
1	0	0	0

04

$T_A = \bar{B}X + B\bar{X}$ $\quad T_B = AB + BX + AX$ $\quad Y = A\bar{X} + \bar{A}\bar{B}X$

Design of sequential ckt & its o/p dia. → 2 + 2 = 12

10(a) basic structure & explanation of PROMs and EPROM | 4+4+5 | 13

(b) (1) Read only & Read write memory (2) Flash | 2+3+2 | 07