CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - IV

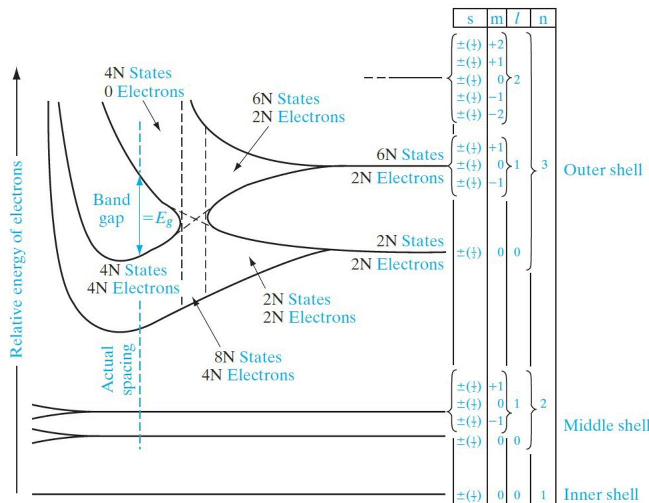
Sub:	Electronic Devices							Code:	18EC33
Date:	15/03/2022	Duration:	90 mins	Max Marks:	50	Sem:	III	Branch:	ECE-A,B,C,D
Answer for 100 marks									

		Marks	OBE CO	OBE RBT
1.	With a neat diagram describe the formation of different energy levels in silicon atom as a function of inter atomic spacing. What are direct and indirect semiconductors?	[5+5]	CO1	L1
2.	Write notes on: (i) intrinsic semiconductor (ii) extrinsic semiconductor (iii) impurity scattering (iv) lattice scattering.	[10]	CO1	L1
3.	Explain the effect of frequency on gate voltage of a MOS capacitor with a P-type substrate	[10]	CO2	L1
4a).	Derive the expression of current density in a semiconductor in terms of charge, carrier concentration, mobility and applied electric field.	[5]	CO1	L2
b)	For a Si bar having a length of 4 μm, doped n-type at $10^{17}/cm^3$, calculate the current for an applied voltage of 2 V with area of $0.01 cm^2$. If the voltage is now raised at 100 V, what will be the change in current? Electron mobility is 1350 $cm^2/V-sec$, for higher field saturation, the velocity for electron is $V_C = 10^7\ cm/sec$.	[5]		
5a).	What is Hall Effect?	[5]	CO1	L2
b)	Semiconductor bar with $w = 0.1\ mm$, $t = 10\ \mu m$, and $L = 5\ mm$ with the length along x axis for $\boldsymbol{B}$=10 kG in z direction ($1\ kG = 10^{-5}\ Wb/cm^2$) and a current of 1 mA along x-direction. Given that $V_{AB} = -2\ mV$, $V_{CD} = 100\ mV$. Find the type, concentration, and mobility of the majority carriers. Consider the thickness to be along z-direction.	[5]		
6.	Explain the various bonding forces in solid. Also differentiate between metals, semiconductors and insulators.	[10]	CO2	L1
7.	Explain two terminal MOS structure with energy band diagram	[10]	CO1	L1
8.	What is metallization process? With neat diagram explain all steps in the fabrication of P-N Junction.	[10]		
9.	Draw and explain I-V Characteristics of n channel PNJFET for different biasing voltages	[10]		
10.	Discuss about photolithography process.	[10]		
11.	Explain the operation of p-channel enhancement mode MOSFET with neat diagrams and Equations.	[10]		

Solution

Q1. As the spacing between the two atoms becomes smaller, electron wave functions begin to overlap.

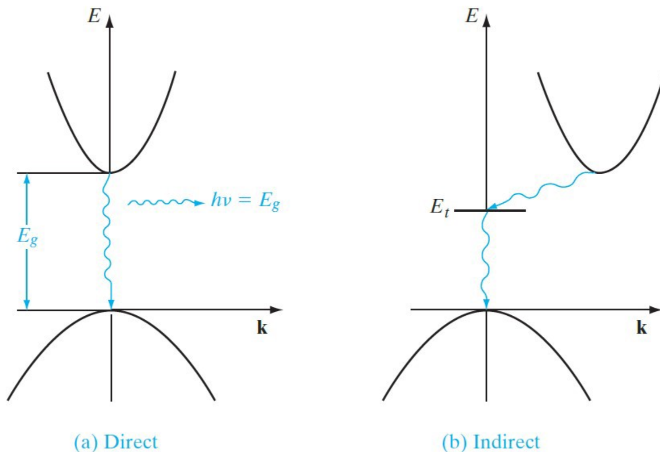
- There is a splitting of the discrete energy levels of the isolated atoms into new levels belonging to the pair rather than to individual atoms.
- In a solid, many atoms are brought together, so that the split energy levels form essentially continuous bands of energies.
- Consider the imaginary formation of a silicon crystal from isolated silicon atoms (N).
- If we consider N Si atoms, there will be 2N, 2N, 6N, 2N, and 6N states of type 1s, 2s, 2p, 3s, and 3p, respectively.
- As the interatomic spacing decreases, these energy levels split into bands.
- The “3s” and “3p” bands grow and merge into a single band composed of a mixture of energy levels.
- At equilibrium this band splits in to valance band and conduction band separated by wide energy gap (Forbidden gap)
- Initially 4N(2N+2N) electrons and 8N states are available. As distance ↓ energy levels split into CB and VB. 4N electrons occupy 4N states in VB and 4N states in CB are empty.
- At 0 K, every state in the valence band will be filled, while the conduction band will be completely empty of electrons.



- Direct Semiconductors: The minimum of the conduction band and the maximum of valence band occur for same value of k.
- Thus an electron making a smallest energy transition from the conduction band to valence band without a change in k value.
- Thus electrons make smallest-energy transition
- There is direct band-to-band transition in direct semiconductors.
- During the transition they radiate light energy.
- Applications: Used for LEDs, Laser
- For GaAs the minimum of the conduction band and the maximum of the valence band occur for same value of k =0.
- The band diagram shown during this discussion are cumbersome to draw in analyzing devices. Therefore band diagram discussed during classification of elements are used.
- Indirect Semiconductor: In Indirect Semiconductors the minimum of the conduction band does not occur at the same k value as the valence band is maximum.
- An electron promoted to the conduction band requires a change of its momentum to make the transition to the valence band
- Si has its valance band maximum at a different value of k than its conduction band minimum.

So the transition from minimum point in conduction band to maximum point in valance band requires some change in k.

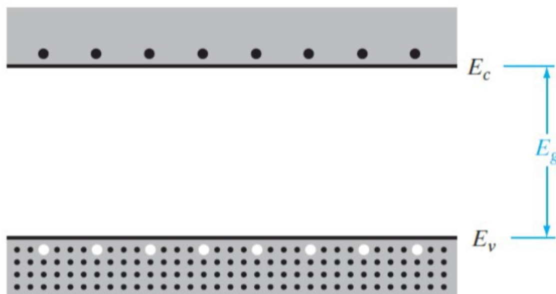
- This change in k requires change in momentum of electron.
- So there is no direct band-to-band transition in Si, it must undergo a change in momentum as well as changing its energy.
- It may go through defect state.



(a) Direct (b) Indirect

Q.2. i) Intrinsic semiconductor:

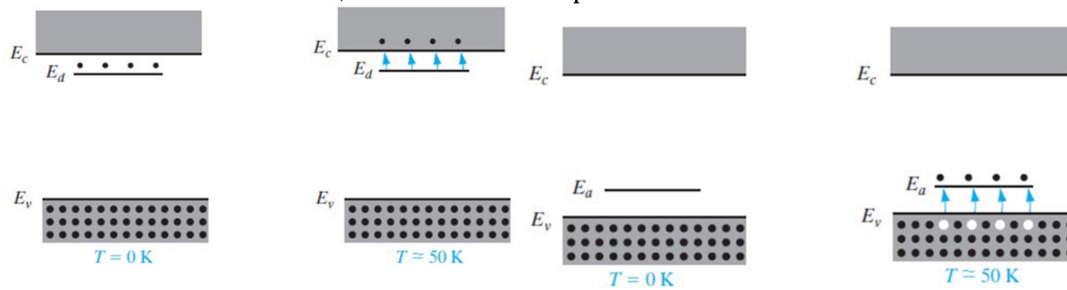
- A perfect semiconductor without any lattice defects is called an intrinsic semiconductor.
- There are no charge carriers at 0K. At higher temps EHPs are generated which are the only charge carriers.
- Since EHP are created in pair, if the 'n' number of electron concentration (electrons/cm^3) in the conduction band which equals to the 'p' number of hole concentration in the valence band are created. i.e. $n=p=n_i$
- Conductivity in a semiconductor depends on two factors
  1. Concentration of electrons and holes. Denoted as n and p and are temperature dependent.
  2. Ability of the electron and holes to travel in the lattice without scattering



ii) An extrinsic semiconductor is a semiconductor doped by a specific impurity to increase the carrier concentration. Thus there are two types of doped semiconductors, n-type (Major electrons) and ptype (Major holes).

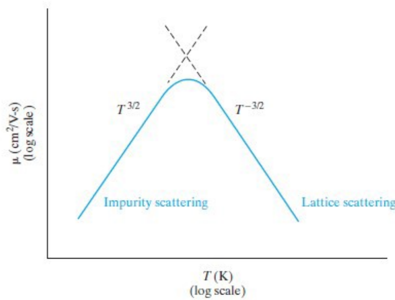
- A n-type semiconductor is created when pentavalent elements P(15), As(33), Sb(51) are used to dope pure semiconductors, like Si and Ge. The impurity atoms are called Donor atoms, since they donate electrons. Thus at about 50–100 K virtually all of the electrons in the impurity level are "donated" to the conduction band. Such an impurity level is called a donor level
- A p-type semiconductor is created when trivalent elements B(5), Al(13), Ga(31)and In(49) are used to dope pure semiconductors, like Si and Ge. When a trivalent atom takes the place of a Si atom, three of its electrons bond with three neighboring Si atoms. However, there is no electron to bond with the fourth Si atom. This leads to a hole or a vacancy between the trivalent and the fourth silicon atom. At low temperatures, enough thermal energy is available to excite electrons from the valence band into the

impurity level, leaving behind holes in the valence band. Since this type of impurity level "accepts" electrons from the valence band, it is called an acceptor level.



iii) Lattice scattering →scattering by vibration of lattice resulting from temperature. Frequency of scattering ↑by ↑in temperature. Results in mobility↓.
iv) Impurity scattering: Scattering from crystal defects such as ionized impurities becomes the dominant mechanism at low temperatures. Impurity scattering events cause a decrease in mobility with decreasing temperature. With a donor doping concentration of 10^{17} cm^{-3}, however, μ_n is 700 cm^2/(V-s). Thus, the presence of the 10^{17}ionized donors/cm^3 introduces a significant amount of impurity scattering.

- As the concentration of impurities increases, the effects of impurity scattering are felt at higher temperatures. The mobilities due to two or more scattering mechanisms add inversely.



Q3 There are three operating conditions of interest in the MOS capacitor: accumulation, depletion, and inversion.

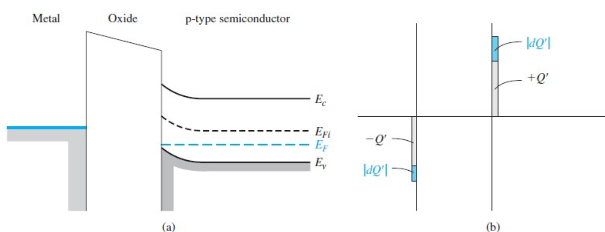


Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

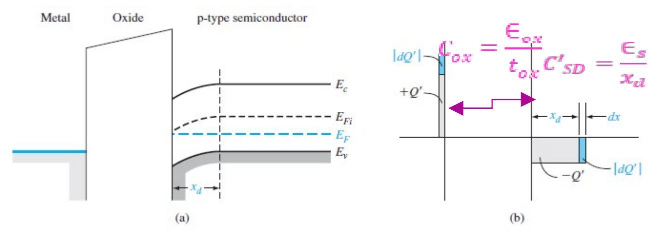


Figure 10.24 | (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

- Small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in the hole accumulation charge Fig 10.23.
- The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor.
- $C'(acc)=C_{ox}=\frac{\epsilon_{ox}}{t_{ox}}$
- Application of a small positive voltage to the gate, induces a space charge region in the semiconductor;Fig 10.24
- A small differential change in voltage across the capacitor will cause a differential change in the space charge width.
- The oxide capacitance and the capacitance of the depletion region now are in series.

$\therefore C'(depl) = \frac{\epsilon_{ox}}{t_{ox}+\left(\epsilon_{ox}/\epsilon_s\right)x_d}$ As the space charge width increases, the total capacitance *C'(depl)* decreases

- We can define the threshold inversion point it is the condition when the maximum depletion width is reached $C'_{min} = \frac{\epsilon_{ox}}{t_{ox}+\left(\epsilon_{ox}/\epsilon_s\right)x_{dT}}$
- In the ideal case, a small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density.Fig 10.25
- The space charge width does not change.
- If the inversion charge can respond to the change in capacitor voltage as indicated in this figure here then $C' = C_{ox}$.

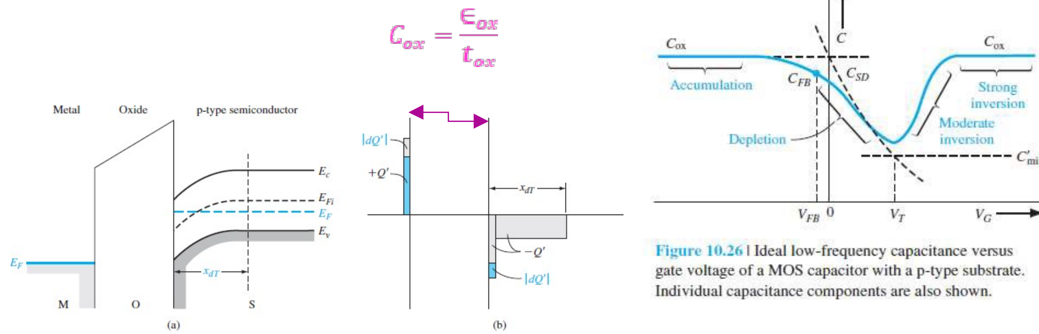


Figure 10.26 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

- Figure 10.25 | (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

The three dashed segments correspond to the three components Cox, C'_{SD} , and C'min.Fig 10.26

- The solid curve is the ideal net capacitance of the MOS capacitor.
- Moderate inversion is the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.
- The point on the curve that corresponds to the flat-band condition is of interest.

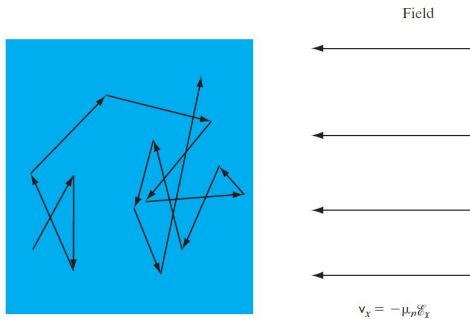
- The flat-band condition occurs between the accumulation and depletion conditions.

$$\therefore C'(FB) = \frac{\epsilon_{ox}}{t_{ox} + \left(\epsilon_{ox}/\epsilon_s\right)\sqrt{\left(\frac{kT}{q}\right)\left(\frac{\epsilon_s}{qN_a}\right)}}$$

- The capacitance at flat band is given by
- We may note that the flat-band capacitance is a function of oxide thickness as well as semiconductor doping.

Q.4.a) If electric field E_x is applied each e_{-n} experiences the force $-qE_x$ Net motion of all electrons is in direction of x.

- If P_x the total momentum of all group electrons in the x direction
- The force of electric field experienced by n electrons $-q\,nE_x = dp_x/dx$.
- To find total rate of change in momentum we must investigate collision probabilities.
- For random collisions → constant probability of collisions.
- Assume group of N_0 no. of electrons at time t=0.· Assume N(t) no. of electrons does not take part in collision by time t



$$-\frac{dN(t)}{dt} = \frac{1}{\bar{t}}N(t)$$

where $\bar{t}^{-1}$ is a constant of proportionality.

The solution of this equation is is mean time between scattering events.
The probability that any electron has a collision in the time interval dt is dt/t.

- Thus the differential change in momentum Px due to collisions in time dt is
-
- The rate of change of Px due to the decelerating effect of collisions is
-
- The sum of acceleration and deceleration effects must be zero for steady state.
- .
- The average momentum per electron
-
- The average a constant net velocity in the negative x-direction
-
- This drift speed is usually much smaller than the random speed due to the thermal motion.
- The current density resulting from this net drift is just the number of electrons crossing a unit area per unit time. $J_x = -qn\langle v_x \rangle$

$$J_x = \frac{nq^2\bar{t}}{m_n^*}\mathscr{E}_x \qquad J_x = \sigma\mathscr{E}_x, \quad \text{where } \sigma \equiv \frac{nq^2\bar{t}}{m_n^*}$$

The conductivity $\sigma(\Omega\text{-cm})^{-1}$ can be written

$$\sigma = qn\mu_n, \quad \text{where } \mu_n \equiv \frac{q\bar{t}}{m_n^*}$$

Q4.b.)

Given L=4 μm, A=0.01 cm^2,n=10^{17} cm^{-3}, V= 2 V

$I = A \cdot J = A.(qnv)$ $\therefore \varepsilon = \frac{V}{L}$ $\therefore \varepsilon = \frac{2}{4 \times 10^{-4}} = 0.5\times10^4\ V/cm$

Drift velocity= $1350 \times 0.5 \times 10^{-4}$. $v = 6.75 \times 10^6$cm/s

$\therefore I = A.(qnv) = 1\times10^{-2} \cdot 1.6\times10^{-19} \cdot 10^{17} \cdot 6.75 \times 10^6$.

$\therefore I = 1080A$

Voltage is increased $\varepsilon = 100V/4 \times 10^{-4}$ cm,

$\varepsilon = 2.5 \times 10^5$ V/cm

$\therefore$Drift velocity $v = 10^7$cm/s

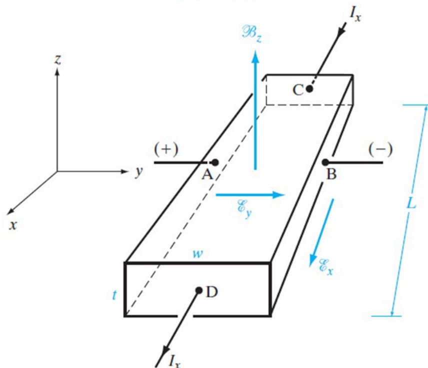
$\therefore I = A.(qnv) = 1\times10^{-2} \cdot 1.6\times10^{-19} \cdot 10^{17} \cdot 10^7$.

$\therefore I = 10800A$

Increase in Voltage cause in increase current.

Q.5. The Hall effect is the production of voltage difference (the Hall voltage) across a current carrying conductor (in the presence of magnetic field), perpendicular to both current and the field. In the y-direction the force is

$$F_y = q(\varepsilon_y - v_x \mathcal{B}_z)$$



- An electric field and voltage V_{AB} is established along the width of the bar
- This is called as Hall Effect.
- The Hall Field is proportional to product of current density and magnetic flux density.
- To maintain a steady state flow of holes F_y must be zero. $\mathscr{E}_y = v_x \mathcal{B}_z$
- V_{AB} is the Hall voltage established. $V_{AB} = \mathscr{E}_y w$
- Now for holes, the current density is given by $J_x = q p_0 v_x$

$$\mathscr{E}_y = \frac{J_x}{qp_0}\mathcal{B}_z = R_H J_x \mathcal{B}_z, \quad R_H \equiv \frac{1}{qp_0}$$

- We see that the Hall Field is proportional to product of current density and magnetic flux density.

5.b.

W=0.01cm, t=10×10^{-4}cm, $\mathcal{B}_z = 10^{-4}$Wb/cm^2 L=0.6cm, I_x=1×10^{-3}A,
V_{AB}=-2×10^{-3} V, V_{CD}=100×10^{-3}V.

From sign we can say that majority carriers are electrons.

$$\therefore n_0 = \frac{I_x}{qtV_{AB}}\mathcal{B}_z = \frac{(10^{-3})(10^{-4})}{1.6\times10^{-19}(10^{-3})2\times10^{-3}}$$

$$\therefore n_0 = 3.125\times10^{17} cm^{-3}$$

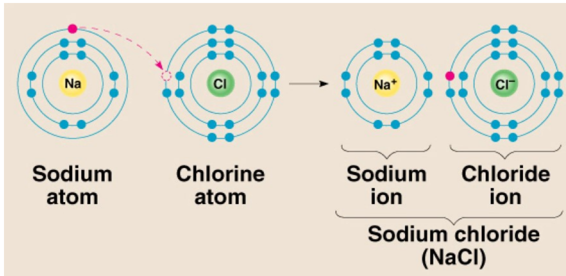
$$\therefore \rho = \frac{V_{CD}/I_x}{L/wt} = \frac{(0.1)/(10^{-3})}{0.5/(0.01)\cdot(10^{-3})} = 2\times10^{-3}$$

$$\mu_n = \frac{\sigma}{qn_0} = \frac{1}{\rho q n_0} = \frac{1}{(2\times10^{-3})(1.6\times10^{-19})3.125\times10^{17}}$$

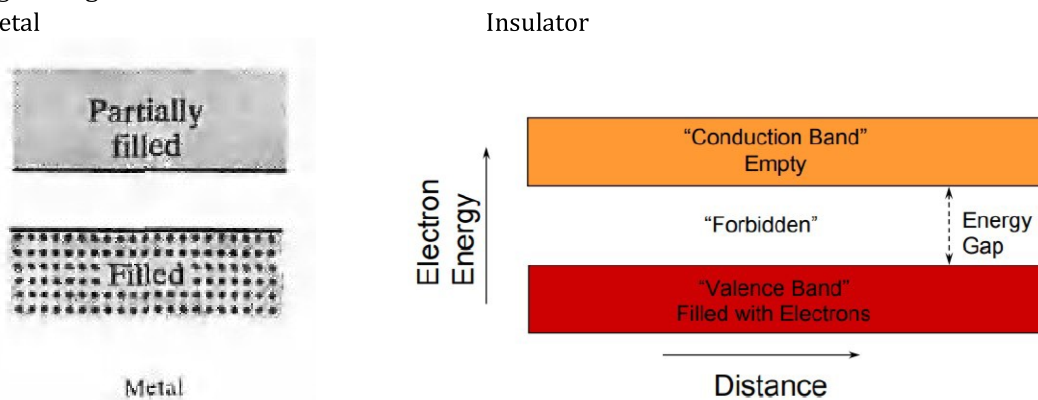
$$\mu_n = 10000 cm^2/(V-s)$$

Q.6. Major Types of bonding forces

- Ionic Bonding: Forms ionic compounds. Transfer of electron takes place. Electrons are transferred between valence shells of atoms. Ionic compounds are made of ions, not molecules. Ionic compounds are called salts or crystals. A typical example of an ionic bond in Sodium chloride (NaCl). Each Na+ ion exerts attractive force on neighboring Cl- ions. In the lattice NaCl structure all electrons are tightly bound to the atoms.



· Metallic Bonding: Bonds formed in metals. Holds the atoms strongly. There is a cloud of electrons around the atoms. Good conductors of electricity. Example: Na, Fe, Al, Cu etc.
· There are complicated differences in the bonding forces for various metals, as evidenced by the wide range of melting temperatures. Mercury Hg(80) 234 K, Tungston W(74)3643 K.
· Covalent Bonding: In covalent bonds pairs of electrons are shared between atoms. They are formed between non-metal atoms The electro negativity difference of the atoms should be <1.7. They form poly atomic ions.
Some key features are: Between nonmetallic elements of similar electro negativity. Formed by sharing electron pairs. Stable non-ionizing particles, they are not conductors at any state
Examples; O_2, CO_2, H_2
Metals, Semiconductors, Insulators.
· An energy band is a range of allowed electron energies. Every solid has its own characteristic energy band structure. The band structure is responsible for the electrical characteristics. We have valence band and conduction band. The energy gap in between is the forbidden gap.
· The energy band in a metal is only partially filled with electrons. Metals have overlapping valence and conduction bands. For an electron to become free to conduct, it must be promoted into an empty available energy state. For metals, these empty states are adjacent to the filled states. Generally, energy supplied by an electric field is enough to stimulate electrons into an empty state. Hence, metals are said to have high conductivity
· Eg. Cu, Ag, Au etc
· Metal Insulator



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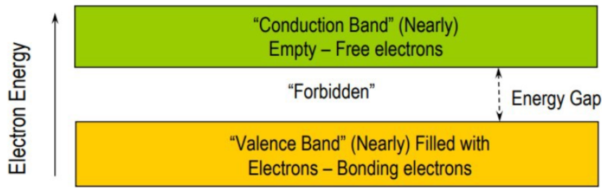
· Insulators: The valence band and conduction band are separated by a large (> 4eV) energy gap, which is a "forbidden" range of energies. Electrons must be promoted across the energy gap to conduct, but the energy gap is large. So small electric fields are not sufficient to transfer the electrons from valence band to conduction band. When the electric field is very large, then the insulation "breaks down" and starts conducting. e.g. Diamond with band gap 5eV, Silicon dioxide
SiO_2 has band gap of 9.0 eV.

· Semiconductor:



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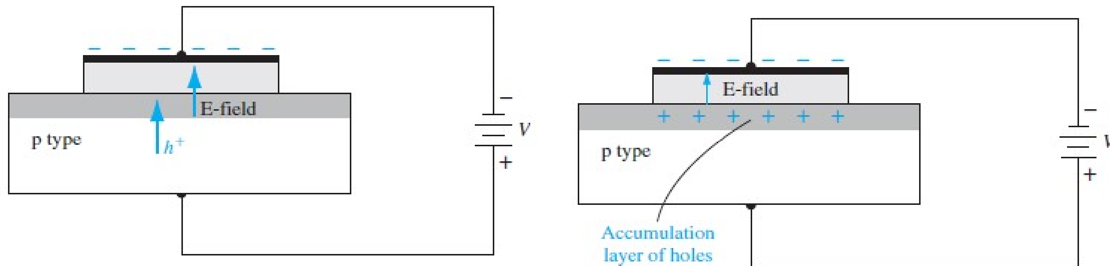
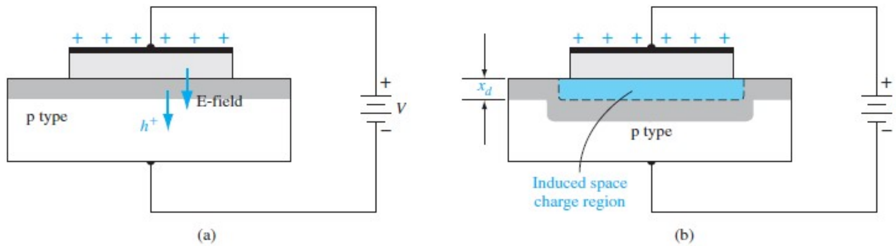
· They belong to group IV in the periodic table. Semiconductors have resistivities in between those of metals and insulators. If relatively few electrons reside in an otherwise empty band, plenty of unoccupied energy states are available into which electrons can move. If we consider Si, valence band is completely full at 0K and conduction band is empty. Since VB is full, no empty states. So no electron transfer. Since conduction band is empty, no charge transport here also. Hence, Si has high resistivity. In Si band gap is 1.1 eV.
Since band gap is low, electrons can be transferred from lower energy valence band by thermal or optical energy. At room temp, Si will have significant number of electrons excited thermally into conduction band, whereas in an insulator (gap > 4ev) negligible electrons in conduction band.
Q7.



- An electric field will be induced with the direction shown.
- The majority carrier holes would experience a force toward the oxide– semiconductor interface.
- An *accumulation layer* of holes at the oxide–semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.



- Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.
- If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a force away from the oxide–semiconductor interface.
- A negative space charge region is created because of the fixed ionized acceptor atoms.
- The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor.
- With zero bias the energy bands in the semiconductor are flat indicating no net charge exists in the semiconductor. This condition is known as *flat band*
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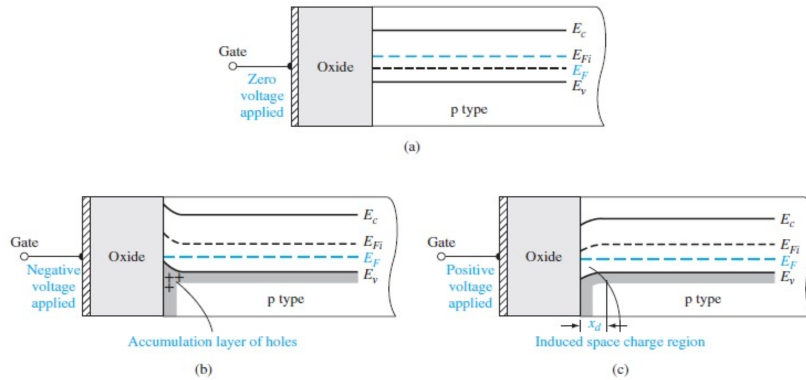


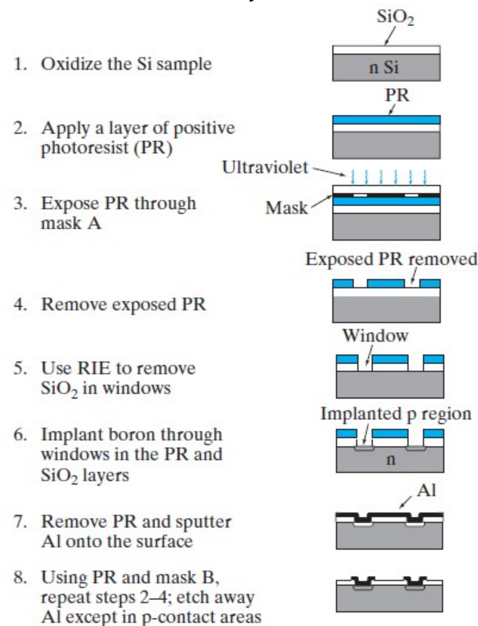
Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias.

- When a negative bias is applied to the gate.
- The valence-band edge is closer to the Fermi level at the oxide–semiconductor interface than in the bulk material
- When a positive voltage is applied to the gate the conduction- and valence-band edges bend as shown in the figure 10.4c, indicating a space charge region similar to that in a pn junction.
- The conduction band and intrinsic Fermi levels move closer to the Fermi level. The induced space charge width is x_d.
- If still larger positive voltage is applied to the top metal gate of the MOS capacitor.
- A larger negative charge in the MOS capacitor implies a larger induced space charge region and more band bending.
- The intrinsic Fermi level at the surface is now below the Fermi level see the figure in next slide.

Q.8. The semiconductor devices are connected to each other through metallization.

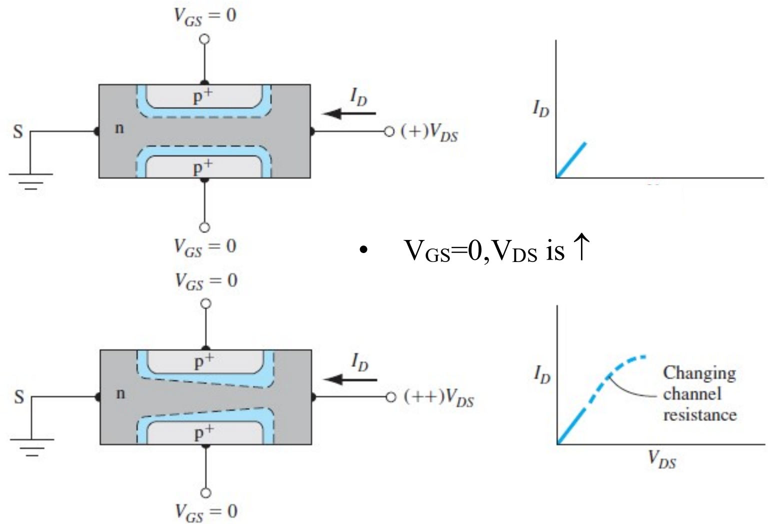
- Metal films are generally deposited by 2 techniques:
  - (i) **physical vapor deposition** technique such as evaporation (e.g., *Au on GaAs*)
  - (ii) **sputtering** (e.g., *Al on Si*)
- Sputtering of ***Al*** is achieved by immersing an ***Al*** target in ***Ar plasma.*** Argon ions bombard the ***Al*** and physically dislodge ***Al atoms*** by momentum transfer. Many of the ***Al atoms*** ejected from the target deposit on the ***Si wafers*** held in close proximity to the target.

Fabrication of P-N Junction



Q.9. Consider the situation in which the gate voltage is held at zero volts, $V_{GS} = 0$, and the drain voltage changes.

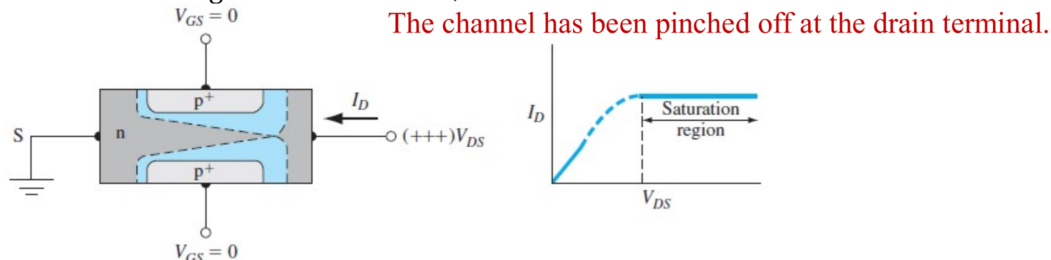
- As the drain voltage ↑ (positive), the gate to- channel pn junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel.
- Zero gate voltage and a small drain voltage.
-



- $V_{GS}=0, V_{DS}$ is ↑

- The effective channel resistance now varies along the channel length.
- Since the channel current must be constant, the voltage drop through the channel becomes dependent on position.
- If the drain voltage increases further,

The channel has been pinched off at the drain terminal.



The drain voltage at pinch off is referred to as $V_{DS(\text{sat})}$.

- For $V_{DS} > V_{DS}(\text{sat})$, the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_{DS}.

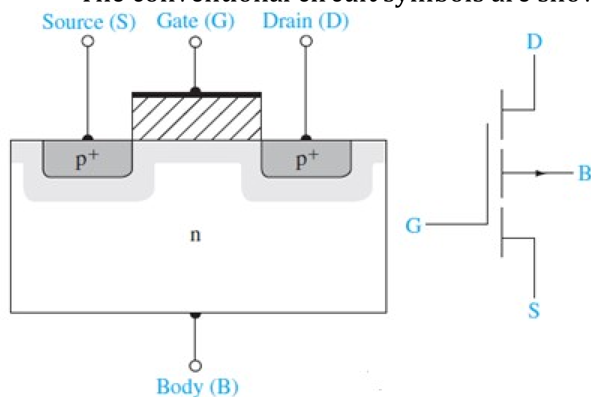
Q. 10. Patterns corresponding to complex circuitry are formed on a wafer using ***photolithography*.**

- First a ***reticle is generated*** which is a transparent silica (quartz) plate containing the pattern corresponding to single chip, opaque regions on the mask are made up of an *UV light-absorbing layer*, like ir**on oxide**.
- Reticle contains the patterns corresponding to a single *chip/die,* created by a computer-controlled electron beam driven by the circuit layout data, using pattern generation software.
- A thin layer of ***electron beam resist*** is placed on the iron-oxide–covered quartz plate, and the resist is exposed by the electron beam to undergo chemical changes.
- After exposure, the resist is *developed* in a chemical solution.
- The developer is used to remove either the exposed (*positive* resist) or the unexposed (*negative* resist) material.
- The iron oxide layer is then selectively etched off in a plasma to generate the appropriate patterns.
- Reticle can be used repeatedly to pattern Si wafers.

- To make a typical integrated circuit, a dozen or more reticles are required, corresponding to different process steps.
- ***Generate reticle. Si*** wafers are first covered with an UV light-sensitive organic material or photo emulsion called ***photoresist.***
- Light shines on the resist-covered wafer through the reticle, causing the exposed regions to become acidified.
- Exposed wafers are developed in a basic solution of ***NaOH***, causing the exposed resist to etch away. Remaining resist is cured by baking at ***125°C*** to harden it.
- After the photo exposure, the wafer mechanically translates on a precisely controlled *x-y* translation stage to the next die location and is exposed again

Q11. In the p-channel enhancement mode device, a negative gate voltage must be applied to create an inversion layer of holes that will "connect" the p-type source and drain regions.

- Holes flow from the source to the drain, so the conventional current will enter the source and leave the drain.
- A p-channel region exists in the depletion mode device even with zero gate voltage.
- The conventional circuit symbols are shown in the figure.



- In the non-saturation region current I_D shall be expressed as $I_D = \frac{k'_p}{2}\frac{W}{L}[2(V_{SG} + V_T)V_{SD} - V_{SD}^2]$
- k'_p=*process conduction parameter*
- Or $I_D = K_p[2(V_{SG} + V_T)V_{SD} - V_{SD}^2]$ In this K_p=*conduction parameter*
- In the saturation region current I_D shall be expressed as $I_D = \frac{k'_p}{2}\frac{W}{L}[(V_{SG} + V_T)^2]$
- Or $I_D = K_p[(V_{SG} + V_T)^2]$